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Objective Data Sheet

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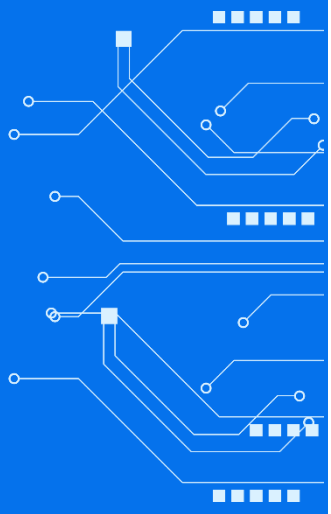
ICL111A

Smart mmWave Sensor Series



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ICL111A

1 General Description

The ICL111A is an Antenna-in-Package (AiP) device with integrated mmWave SoC based on FMCW radar transceiver technology. It operates within the 24 GHz K-band, supporting modulation bandwidths of up to 1 GHz in each individual frequency-sweeping chirp.

The ICL111A is a fully integrated SoC that encompasses all critical mmWave functions, including a TX/RX antenna, full transceiver, signal processing path, K-band RF transceiver, on-chip pattern generator, PLL, and ADCs. The pattern generator supports three frequency sweeping modes with different time-frequency waveforms, i.e. continuous wave, saw-tooth, and triangular waveforms. The pattern generator and PLL support fast chirp mode up to 8 kHz chirp rate. The digitized signals from the receiver chain can be serialized via multiple output interfaces.

The ICL111A adopts a compact FCCSP package measuring 5.5 mm × 5.5 mm and featuring 28 bumps.

2 Main Features

- 24 GHz All-in-one FMCW radar sensor with fully integrated antennas, radio, and digital baseband
- Compact size antenna on package
- Up to 1 GHz bandwidth FM tuning range
- One transmit channel and one receive channel
- Low power consumption: Operates at 55 μA current with a 0.3% duty cycle, generating 1 chirp per second
- Phase noise: -97 dBc/Hz @ 1 MHz
- Built-in 2.5 MHz conversion rate ADC with 16 bits resolution
- Fast FMCW chirp ramp rate: up to 20 MHz/μs
- High FMCW chirp linearity, achieving 0.45‰ with a 250 MHz tuning range
- Enhanced precision in TX power through on-chip power detector and temperature sensor
- Built-in hardware accelerator, support complex FFT and CFAR function
- Detection applications supported without the need for external MCU supporting
- Configuration interface support: I2C/SPI/UART
- Data output interface support: GPIO/SPI (master/slave mode)/UART
- Support flexible power supply modes
- Simplified hardware design with an ultra-compact 5.5 mm × 5.5 mm FCCSP package for PCB
- Junction temperature range: –40ºC to 105ºC

3 Applications

- Smart Home Radar Sensor
- Smart Lock / Ring Bell
- Proximity and Position Sensor
- Home Appliance Radar Sensor
- Motion Detector
- Gesture Recognition

Table of Contents

4 Block Diagram

This product utilizes a single antenna patch for both transmitting and receiving functions.

The RF and analog subsystem implements the FMCW (frequency-modulated continuous-wave) transceiver system with integrated TX/RX antenna, synthesizer, mixer, and baseband. Gain controls are applied to both transmitter and receiver to adjust the whole link budget to work in different scenarios. The baseband includes inter-mediate frequency (IF) programmable amplifier, filters, and ADCs. A built-in DSP accelerator can process the IQ ADC's raw data with Range FFT or Doppler FFT.

The ICL111A offers configurable settings via the I2C/SPI/UART interface, allowing for direct output of DS RAW data and serialization of DSP processed data via the SPI/UART interface.

Figure 4-1 presents the design of the ICL111A.

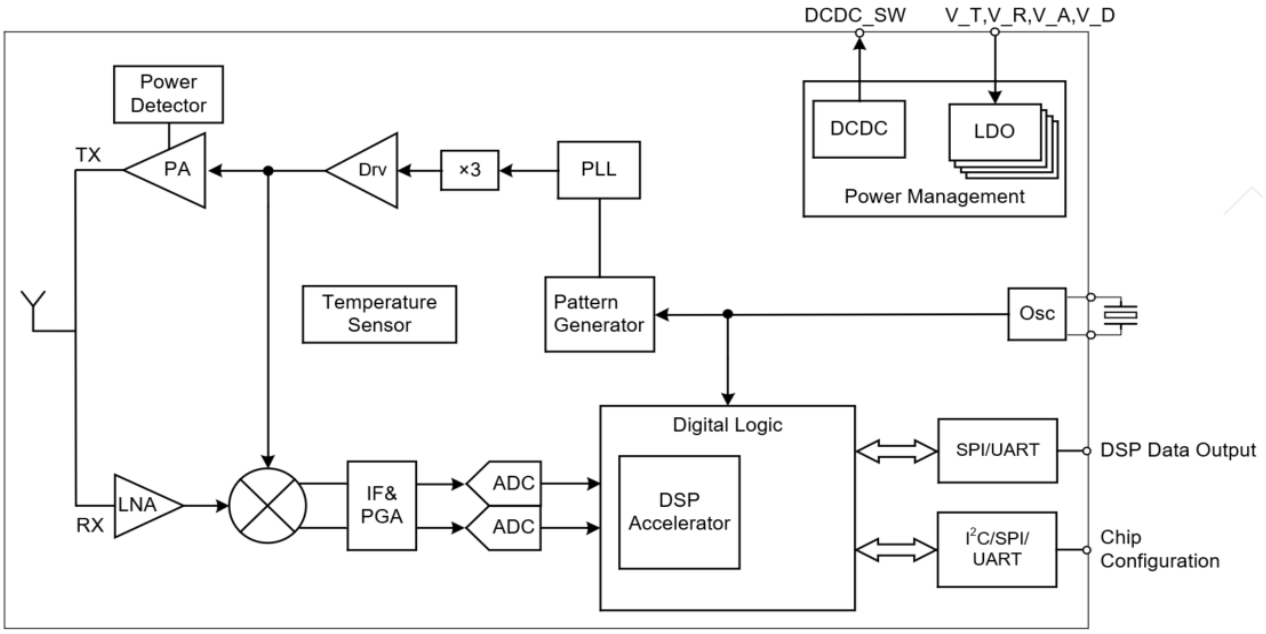


Figure 4-1 ICL111A block diagram

5 Terminal Configuration and Description

5.1 Pin Diagram

The outlook of the ICL111A is shown in Figure 5-1.

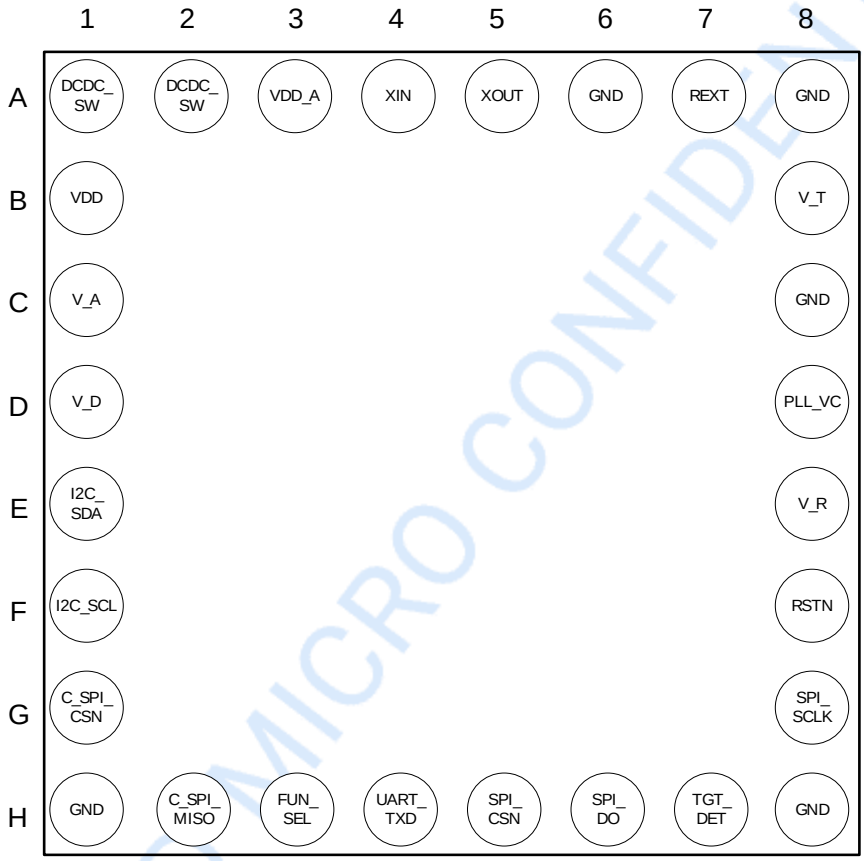


Figure 5-1 Pin diagram (top view)

5.2 Signal Descriptions

Information of each pin is given in Table 5-1.

Table 5-1 Pin descriptions

Pin Name	Ball_No	Type	Description
DCDC_SW	A1, A2	OUT	DCDC regulator switch node. Connect to the power inductor
VDD	B1	Power	3.3 V power supply for the DCDC converter and digital domain
V_A	C1	Power	1.6 V power supply for analog circuits
V_D	D1	Power	1.6 V power supply for digital circuits
I2C_SDA	E1[1]	OD	Configuration_I2C_SDA: Configuration channel I2C data I/O (open drain)
		IN	Configuration_SPI_MOSI: Configuration channel SPI data input
		IN	Configuration_UART_RX: Configuration channel UART receiver
I2C_SCL	F1[1]	IN	Configuration_I2C_SCL: Configuration channel I2C clock
		IN	Configuration_SPI_SCLK: Configuration channel SPI serial clock

		OUT	Configuration_UART_TX: Configuration channel UART transmitter
C_SPI_CSN	G1[1]	IN	Configuration_SPI_CSN: Configuration channel SPI chip select enable
C_SPI_MISO	H2[1]	OUT	Configuration_SPI_MISO: Configuration channel SPI data output
		IN	Chip pin mux function, see Table 5-4
FUN_SEL	H3[1]	IN	Chip pin mux function, see Table 5-4
UART_TXD	H4[1]	IN	Standby mode pin mux function (internally pull down), see Table 5-2
		OUT	DAT_REQ: Data Channel data ready indication at SPI Slave mode
		OUT	DATA_UART_TX: Data Channel UART output
SPI_CSN	H5[1]	OUT/IN	DATA_SPI_CSN: DATA channel SPI chip select enable
		OUT	GPIO Output, Zone Detect 3. High: target exists; Low: no target.
SPI_DO	H6[1]	IN	Configuration channel I2C address high bit configuration, see Table 5-5
		OUT	DATA_SPI_DO: DATA channel SPI data output at RX channel
		OUT	GPIO Output, Zone Detect 0. High: target exists; Low: no target
TGT_DET	H7[1]	IN	Configuration channel I2C address low bit configuration, see Table 5-5
		OUT	GPIO Output, Zone Detect 1. High: target exists; Low: no target
SPI_SCLK	G8[1]	OUT/IN	DATA_SPI_SCLK: DATA channel SPI clock
		OUT	GPIO Output, Zone Detect 2. High: target exists; Low: no target
RSTN	F8	IN	External hardware reset input: A logic LOW on this pin resets the device, causing internal digital circuit to take their default states
V_R	E8	Power	1.6 V analog power supply for RX sections
PLL_VC	D8	IN	Connected to external loop filter to drive the internal VCO
V_T	B8	Power	1.6 V analog power supply for TX sections
REXT	A7	IN	Current bias circuit input, connect to ground with a bias resistor
XOUT	A5	OUT	Crystal oscillator Output port
XIN	A4	IN	Crystal oscillator or external clock Input port
VDD_A	A3	Power	3.3 V power supply for analog domain
GND	A6, A8, C8, H1, H8	GND	Ground

Note:

[1] There are pin multiplexing functions in Pin E1, F1, G1, H2, H3, H4, H5, H6, H7, and G8.

5.3 Work Mode

The ICL111A encompasses four work modes. During the power-up of the ICL111A or the chip settling time following a hardware reset, it is essential to appropriately configure Pin H4/H5/G8 to match the selected configuration status. The mapping between the pin configuration and the chip's work modes is presented in Table 5-2.

Table 5-2 Working Mode Selection Setup

Pin H4	Pin H5	Pin G8	Chip Configuration/Work Mode
Low	-	-	Standby Mode
High	High	Low	Standalone Mode: use case 1

High	Low	High	Standalone Mode: use case 2

5.3.1 Standby Mode

The ICL111A incorporates a standby mode for efficient power management, activating when Pin H4 is configured to a low or floating state during the power-up period (refer to Table 5-2). Upon entering the standby mode, only the power management unit, oscillator unit, and a subset of the digital unit are activated.

This device exits the standby mode when there are changes made to the configuration registers.

5.3.2 Standalone Mode

The ICL111A offers three standalone modes tailored for short-range, mid-range, and long-range detection, respectively. In each of these three modes, the ICL111A can autonomously detect the presence of moving or micro-moving individuals within the designated area. Moreover, each distance detection mode is further subdivided into 2-4 specific distance detection zones, providing users with the flexibility to select the most suitable option according to the specific requirements of their actual application scenarios.

The ICL111A reports detection results using up to 4 IO pins. A high level on these pins signifies the detection of a target within the corresponding range, while a low level indicates no target detected. These pins include SPI_DO (pin H6), TGT_DET (pin H7), SPI_SCLK (pin G8), and SPI_CSN (pin H5), each representing a distinct detection range, ranging from near to far. Table 5-3 outlines a comprehensive description of the three typical use cases for the Standalone Mode.

Table 5-3 Description of the three Standalone Mode use cases

Parameter	Standalone Mode 1	Standalone Mode 2	Unit
Moving Human Detection Range	0~1.5	0~5	m
Motionless Human Detection Range		0~4	m
Field of View	90	120	°
Detection Range of Pin H6	0~0.6	-	m
Detection Range of Pin H7	0~0.9	-	m
Detection Range of Pin G8	0~1.2	0~3.6	m
Detection Range of Pin H5	0~1.5	0~4.9	m
Trigger Delay	0.28	0.25	s
Absence Report Delay	1.96	30	s

5.4 Pin Mux function

The ICL111A features multiple digital communication multiplexing functions on Pin E1, F1, G1, H2, H3, H4, H5, H6, H7, and G8. Specifically, during the power-up of the ICL111A, it is crucial to appropriately configure Pin H2 and H3 to enter the Selected Chip Configuration mode (refer to Table 5-4). The configuration of the data output mode and CFAR function is achieved through the ICL111A's register settings.

Table 5-4 Function mode selection setup - Chip Configuration setting

Pin H2	Pin H3	Chip Configuration Mode
Low	Low	UART
Low	High	I2C
High	Low	SPI
High	High	Reserved

In I2C communication mode, when the chip configuration is set, it is necessary to configure Pin H6 and H7 for setting the slave chip's address during the ICL111A power-up chip settling time. The I2C Configuration mode allows up to 4 devices to share the same I2C bus, refer to Table 5-5 for more details.

Table 5-5 I2C device address

Pin H6	Pin H7	I2C Slave Device Address
Low	Low	7'b010_0000
Low	High	7'b010_0001
High	Low	7'b010_0010
High	High	7'b010_0011

5.5 Chip Configuration

The ICL111A's configuration states are exclusively determined by the external voltage applied to Pin H2, H3, H4, H5, and G8 during the chip settling time. Each pin configuration comprises two states: low and high. A pin can be set to "low" when connected to ground with a 3.3 kΩ resistor, and it can be set to "high" when connected to VDD with a 10 kΩ resistor. Notably, Pin H2 and H3 can be left floating when set to "high" since they are internally pulled up, while Pin H4 can be floated when set to "low" due to its internal pull-down configuration.

Following the chip settling time, it is essential to release the control over the selection of the external applied configuration communication mode on Pin H2, H3, H4, H5, and G8. This allows the chosen pins' configuration communication mode or data communication mode to be triggered effectively.

6 Functional Description

6.1 Transceiver Section

The ICL111A features a single transmitter with customizable parameters accessible through the I2C/SPI/UART configuration channel. The transmitter settings can also be directly managed using the waveform generator. Through the TX port, the transmitter is capable of delivering RF power of up to 12 dBm, and it supports programmable output power for flexible system optimization.

In terms of reception, the ICL111A incorporates a comprehensive receiver module, comprising elements such as LNA, mixer, LPF filters, PGAs, ADCs, and decimation filters. The baseband subsystem is equipped with a quadrature mixer, RX channels' IF, and ADC chains to generate complex I and Q outputs tailored for DSP processing.

6.2 Waveform Generator Section

The waveform generator offers a linear frequency chirp, allowing for a frequency deviation ranging from 0 MHz to 1000 MHz. Additionally, the generator supports Continuous Wave (CW) mode. It is designed to generate a

sequence of frequency chirps with precise timing. Figure 6-1 illustrates the indicative timing for each frequency chirp.

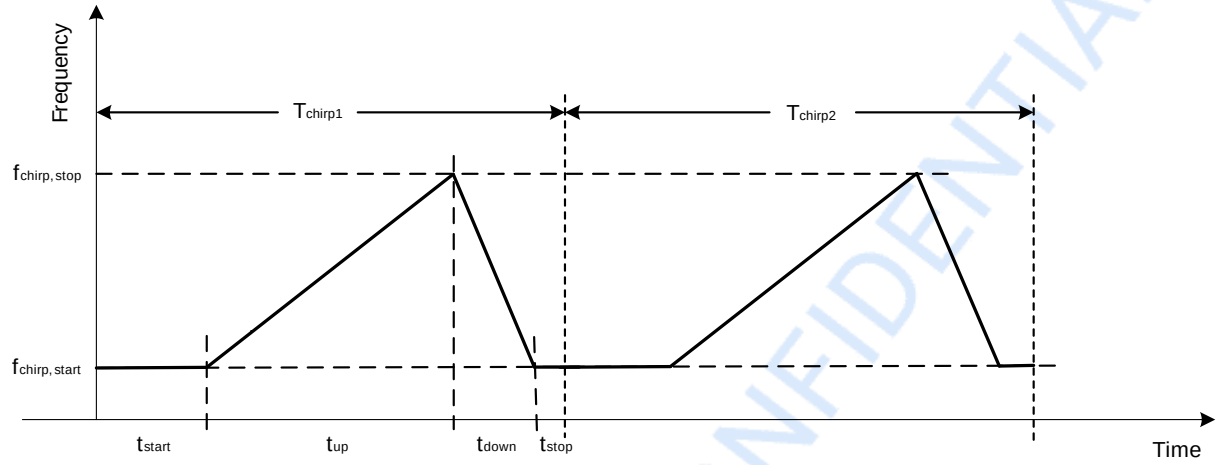


Figure 6-1 Timing parameters in a frequency chirp

The ICL111A works in continuous sensing mode, with each frame commencing at t_{pre}. During this period, the waveform generator initializes to facilitate chirp generation. The duration of t_{pre} is programable, typically set to 20 µs. Subsequently, the TX output port transmits the specified number of chirps for target sensing. Following the completion of the last chirp within a frame, the ICL111A is able to enter a low power mode during the NOP time, as indicated by $t_{\_NOP}$ in Figure 6-2.

When register 0x41 bit 4 is configured to 0, the RF transceiver components (PA, LNA) and the baseband circuits (ADC, LPF&PGA) will enter automatic power-down mode during each frame's NOP time, denoted as $t_{\_NOP}$, and resume operation at the onset of the subsequent t_{pre} period. Within the NOP time, the PD time represents the ICL111A's complete power-down duration. The ICL111A requires a typical $t_{\_2pd}$ time of 22 µs for transitioning to or from low power mode.

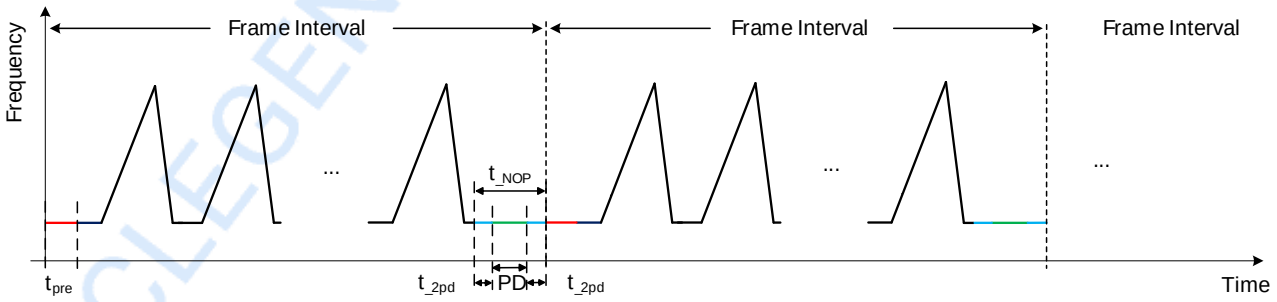


Figure 6-2 Continuous sensing mode

6.3 DSP Accelerator

The ICL111A incorporates Range FFT, Doppler FFT, and DSP acceleration algorithms into its functionality. Figure 6-3 provides a typical DSP flow diagram illustrating the sequence of these integrated processes.

Functional Description

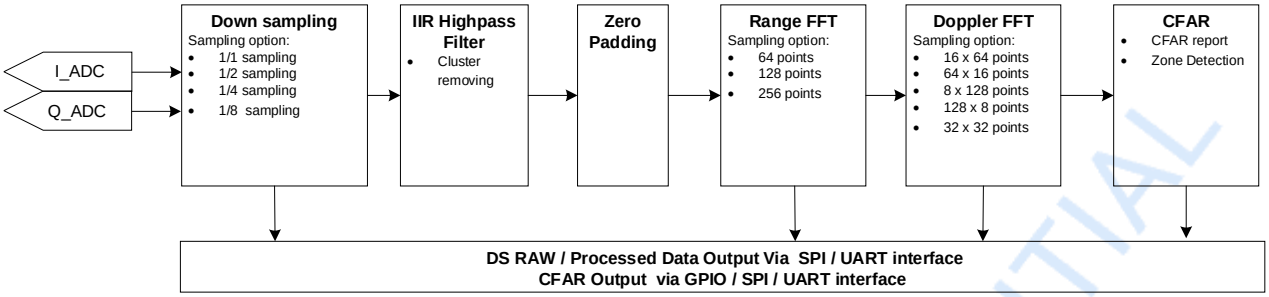


Figure 6-3 DSP accelerator data flow

The hardware accelerator's output can be flexibly chosen from DS RAW data, Range FFT data, Doppler FFT data, or CFAR data through the configuration of the data output format.

The I/Q data output from the RX channel ADCs undergoes processing within the DSP accelerator. Within the hardware accelerator, the raw data undergoes initial down-sampling, with the decimation filter supporting four modes: 1/1, 1/2, 1/4, and 1/8 down-sampling. The down-sampled data can be directed either as DS raw data or routed through the cluster removing filter (IIR High-pass Filter) and Zero padding. The total number of data points in a single chirp is configurable.

For enhanced range accuracy, the zero-padding process can be opted for data interpolation, as depicted in Figure 6-4. The ADC conversion is adjustable to output specific data points, commencing from T0 and concluding at T3. Data Zone 2's information remains unchanged, while the data in Data Zone 1 and Data Zone 3 is set to zero. Subsequently, the cumulative data spanning from Data Zone 1 to Data Zone 3 is forwarded for Range FFT processing.

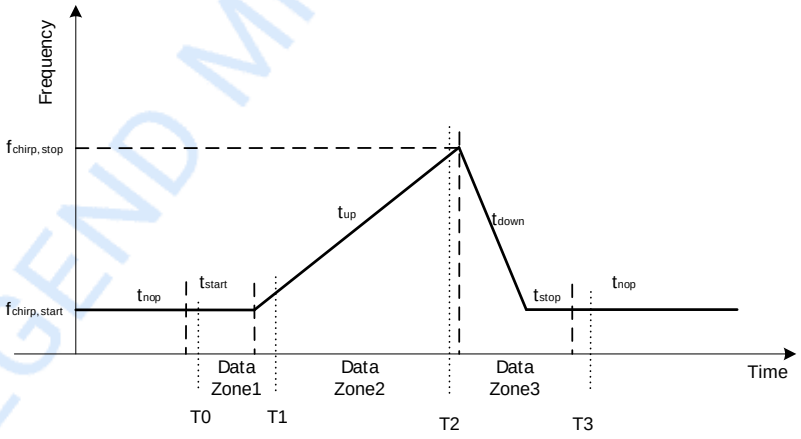


Figure 6-4 Zero padding data sampling diagram

Subsequently, the zero-padded data is directed to the Range FFT processing block, supporting programmable FFT sizes of 64/128/256 points. If Doppler processing is chosen, the output from Range FFT is routed to the Doppler engine. Doppler processing accommodates sampling points in configurations of 16×64, 64×16, 8×128, 128×8, and 32×32. In both Doppler and Range FFT, Hanning, Hamming, Blackman, or rectangular windows, each with corresponding widths, can be applied prior to the transformation. Finally, the CFAR engine can be selected as the concluding optional processing stage.

6.4 CFAR Function

If the CFAR Report function is enabled, CFAR detection is performed based on Doppler FFT data, as shown in Figure 6-3, and the CFAR report data will output via SPI/UART Interface.

When the CFAR Report function is activated, CFAR detection is executed utilizing Doppler FFT data, as illustrated in Figure 6-3. The resulting CFAR report data will be transmitted through the SPI/UART interface.

6.5 Power Supply Section

The ICL111A operates within a 3.3 V power supply domain, relying on a nominal 3.3 V supply voltage available on the PCB board. This 3.3 V supply is transformed into a 1.6 V supply using on-chip DCDC circuits or an external DCDC. The ICL111A accommodates two power supply modes: a single 3.3 V power supply mode and a dual power supply mode (3.3 V and 1.6 V).

For optimal Power Supply Rejection Ratio (PSRR), the 3.3 V power supply domain should be equipped with a 100 nF capacitor positioned as close as possible to the power pins.

The DCDC_SW pin serves as an output pin for the internal DCDC buck converter, and it should be connected to a 22 μH power inductor and a 22 μF capacitor to serve as the internal DCDC's output filter. The power inductor, recommended to be of low Equivalent Series Resistance (ESR) like the SWPA252012S220MT reference, along with the output capacitor, forms a low-pass filter. The use of ceramic capacitors with low ESR in this configuration is advised for minimal output voltage ripple. To maintain resistance at high frequencies and achieve minimal capacitance variation with temperature, it is advisable to employ capacitors with X7R or X5R dielectric.

6.6 Temperature Sensor

The ICL111A incorporates a 10-bit temperature sensor to facilitate temperature monitoring.

6.7 Power detector

The ICL111A is equipped with a 10-bit power detector sensor designed for monitoring transmitter output power. This power detector enables precise control and detection of TX power in the ICL111A. For detailed application information, refer to the *Application Guide for ICL111A Power Detector and Temperature Sensor*.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Table 7-1 Absolute maximum ratings[1]

Parameter	Description	Min.[2]	Max.[2]	Unit
VDD_{max}	3.3 V power supply max input	-0.5	3.7	V
$V\_1.6_{max}$	1.6 V power supply (when internal DCDC is not used) max input	-0.5	3.7	V
RF_IN_{max}	Externally applied power on RX	-	-3.6	dBm
$EIRP_{max}$	Externally applied power on TX	-	15	dBm

Analog Input and Output voltage	Externally applied voltage at PLL_VC, REXT, XIN, XOUT, DCDC_SW ports	-0.5	3.7	V
Digital Input and Output voltage	Externally applied voltage at RSTN, I2C_SDA, I2C_SCL, C_SPI_MOSI, C_SPI_CSN, FUN_SEL, UART_TXD, SPI_CSN, SPI_DO, TGT_DET, SPI_SCLK ports	-0.5	3.7	V
T_J	Junction temperature range	-40	125	°C
T_{STG}	Storage temperature range	-40	125	°C

Note:

[1] All voltages with respect to ground.

[2] Attention: Stresses exceeding those Max. and Min. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

7.2 ESD Ratings

Table 7-2 ESD ratings

Model		Value	Unit
V_{ESD}	HBM: Human body model	+/-2000[1]	V
	CDM: Charge device model	+/-500[2]	V

Note:

[1] According to ANSI/ESDA/JEDEC standard, Method JS-001-2017.

[2] According to ANSI/ESDA/JEDEC standard, Method JS-002-2014.

7.3 Thermal Resistance

Table 7-3 Thermal resistance

Parameter	Description	Min.	Typ.	Max.	Unit
$R_{\theta JA}$[1]	The junction-to-ambient thermal resistance	-	53.6	-	°C/W
$R_{\theta JB}$[2]	The junction-to-board thermal resistance	-	46.8	-	°C/W
$R_{\theta JC}$[3]	The junction-to-case thermal resistance	-	10.3	-	°C/W

Note:

[1] $T_j = T_A + R_{\theta JA} \times P_{total}$, where P_{total} is the power consumption of the chip and T_A is the environment temperature in the still air.

[2] $T_j = T_B + R_{\theta JB} \times P_{total}$, where P_{total} is the power consumption of the chip and T_B is the board temperature in the still air.

[3] $T_j = T_C + R_{\theta JC} \times P_{total}$, where P_{total} is the power consumption of the chip and T_C is the case temperature in the still air.

7.4 Recommended Operating Conditions

Table 7-4 Recommended operating conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD_A	3.3 V power supply for analog circuits	3.0	3.3	3.6	V
VDD	3.3 V power supply for DCDC and digital I/O circuits	3.0	3.3	3.6	V
V_T, V_R, V_A, V_D	1.6 V power supply when the internal DCDC is bypassed	1.5	1.6	1.7	V
VIH	Voltage input High	2.3	-	VDD	V
VIL	Voltage input Low	0	-	0.8	V
VOH	Voltage output High	2.45	-	VDD	V
VOL	Voltage output Low	0	-	0.45	V
T_J	Operating junction temperature range	-40	-	105	°C

7.5 Power Supply Characteristics

7.5.1 Power Supply Modes

The ICL111A features an internal low PSRR DCDC module and is compatible with two power supply modes: a single 3.3 V power supply mode and a dual power supply mode at 3.3 V/1.6 V.

7.5.1.1 3.3 V Single Power Supply Mode

In the 3.3 V single power supply mode, the ICL111A can leverage its internal low PSRR DCDC module by linking VDD_A and VDD to the external 3.3 V power supply, and connecting DCDC_SW to V_T/V_R/V_A/V_D through an inductor.

7.5.1.2 3.3 V/1.6 V Dual Power Supply Mode

In the 3.3 V/1.6 V dual power supply mode, the internal DCDC is bypassed by floating DCDC_SW. VDD_A and VDD are linked to the external 3.3 V power supply, while V_T/V_R/V_A/V_D are connected to the external 1.6 V power supply.

7.5.2 Power Consumption

The data presented in Table 7-5 is obtained at an ambient temperature of 25°C, using a single power supply mode. The applied external voltage corresponds to the typical values provided in Table 7-4.

Table 7-5 Average power consumption

Parameter	Description	Min.	Typ.	Max.	Unit
P_{total}	Average power consumption with the internal DCDC in use, and all the circuits operating in active mode.	-	420	-	mW
$P_{standby}$	Average power consumption with the internal DCDC in use, and all the circuits functioning in standby mode.	-	34	38	mW
$P_{0.3\%dutycycle}$	Average power consumption during operation with a 0.3% duty cycle, generating 1 chirp per second.	-	182	-	μW

The data in Table 7-6 is collected at an ambient temperature of 25°C when the internal DCDC is employed. The applied external voltage corresponds to the typical values provided in Table 7-4.

Table 7-6 Maximum current ratings at power terminals

Parameter	Supply Name	Min.	Typ.	Max.	Unit
Current Consumption	VDD_A	-	-	27	mA
	VDD	-	-	110	mA

The data in Table 7-7 is collected at an ambient temperature of 25°C when the internal DCDC is bypassed.

Table 7-7 Maximum current ratings at power terminals

Parameter	Supply Name	Min.	Typ.	Max.	Unit
Current Consumption	VDD_A	-	-	26	mA
	VDD	-	-	34	mA
	V_T	-	-	83	mA
	V_R	-	-	35	mA
	V_A	-	-	30	mA

	V_D	-	-	6	mA

7.6 Dynamic Performance

Unless stated otherwise, the following conditions prevail: single power supply mode, with VDD and VDDA connected to 3.3 V. T_{case} = 25 °C. The reference plane on the PCB is 1.6 mm from the bump center, and both input and output load impedances are set at 50 Ω. All RF parameters are measured on an application board, and any pertinent details are to be included.

Table 7-8 RF performance

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_out	TX output frequency range	-	24	-	25	GHz
P_{max}_RF_{in}	Max power feed into RX input	-	-	-	-3.6	dBm
f_in	RX frequency range	-	24	-	25	GHz
EIRP	-	-	-	11	14	dBm
NF	RX noise figure	SSB, including antenna, RF and ADC in RX@32.9 dB G_RF_{RX}	9	10.5	-	dB
IP1dB	RX RF Input 1 dB compression point (Rx chain includes ADC and antenna gain)	31 dB gain, 24 GHz	-	-28.5	-	dBm
		25 dB gain, 24 GHz	-	-24.5	-	dBm
G_RF_{RX}	Gain of receiver	Including antenna gain	19	30	34	dB

Table 7-9 Antenna Performance

Parameter	Description	Condition	Min.	Typ.	Max	Unit
Grxa	RX antenna Gain	24 GHz	-	1	-	dBi
Gtxa	TX antenna Gain	24 GHz	-	3.6	-	dBi

Table 7-10 Baseband performance

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Res_ADC	ADC resolution	-	-	16	-	bit
Fs	ADC conversion rate	-	-	2.5	-	MHz

Table 7-11 Pattern generator and PLL performance

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Crystal Frequency	PLL input reference frequency	-	-	25	-	MHz
BW_PLL	PLL bandwidth	-	60	120	240	kHz
PN_{1MHz}	Phase noise at 1 MHz offset @ TX output port	With the off-chip filter parameters as follow: R1=1.6K Ω, C3=2.7nF C4=390 pF (BW_PLL=120 kHz)	-	-97	-91	dBc/Hz
BW_Chirp	FMCW chirp bandwidth	Measured @ TX output	-	0.25	1	GHz
Chirp Rate	FMCW chirp rate	BW_PLL=240 kHz, BW_Chirp=1 GHz	-	-	20	MHz/μs

Freq_err	rms frequency error during FMCW frequency modulation	BW_PLL=240 kHz, BW_Chirp=1 GHz R_Ramp=13 MHz/μs	-	1‰	-
		BW_PLL=240 kHz, BW_Chirp=250 MHz R_Ramp=3.3 MHz/μs	-	0.45‰	-

Table 7-12 DCDC performance

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{sw}	Internal DCDC switching frequency	Single power supply mode	400	500	650	kHz

7.7 Antenna Pattern (Test)

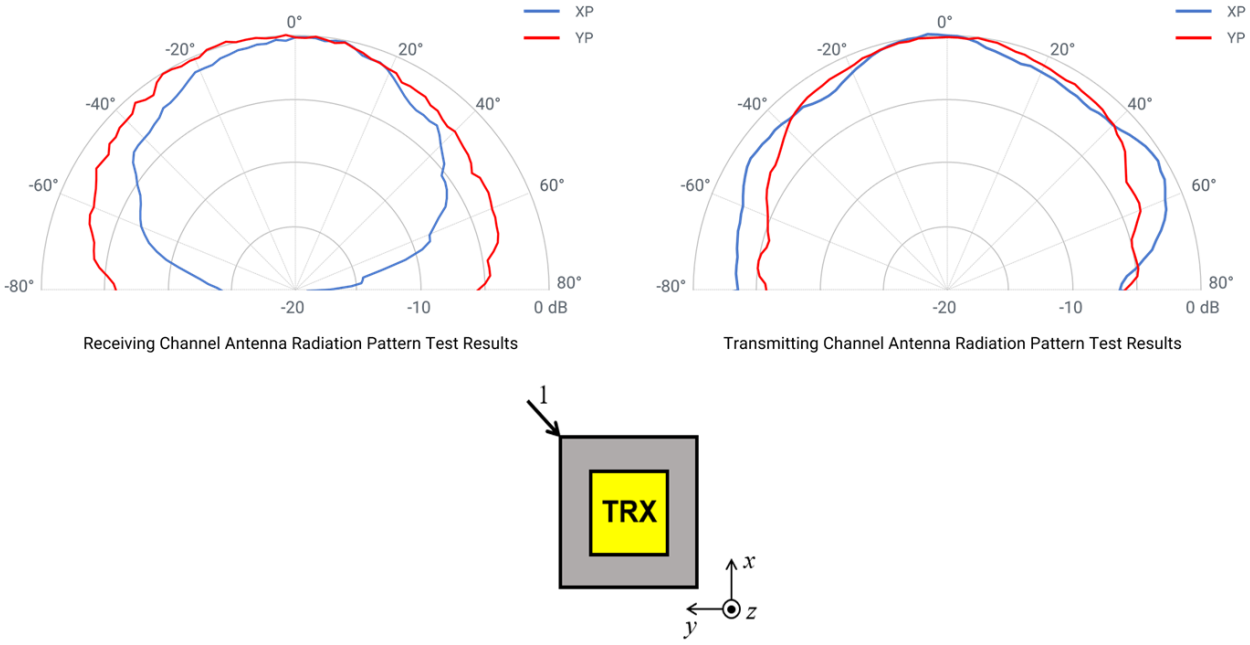


Figure 7-1 Antenna pattern

7.8 Timing and Switching Characteristics

7.8.1 Start-up Sequence

The start-up sequence is illustrated in Figure 7-2. If the ICL111A operates in single power supply mode, the power-up sequence requirements for the power supply pins (as V_T/V_R/V_A/V_D) can be disregarded. This is because these pins receive their supply from the internal DCDC, and the power-up sequences are regulated by the internal power management unit. However, if the ICL111A operates in dual power supply mode, it is essential to power up the V_T, V_R, V_A and V_D pins after VDD, within approximately 1.2 ms. Following a rough time of 3 ms (T_{start}), the crystal oscillator stabilizes. Approximately 0.5 ms after T_{start}, the chip configuration and data communication interfaces become operational, the internal SYS_RSTn is released, the external pin mux function selection control can be released. Subsequently, after around 0.4 ms, the PLL synthesizer is enabled. Finally, in approximately 0.2 ms, all function blocks are ready for operation.

The time duration from the VDD power-up to the release of the external Pin H2, H3, H4, H5, and G8 pin mux function selection control, along with the readiness of chip configuration and data communication, is

approximately 3.5 ms.

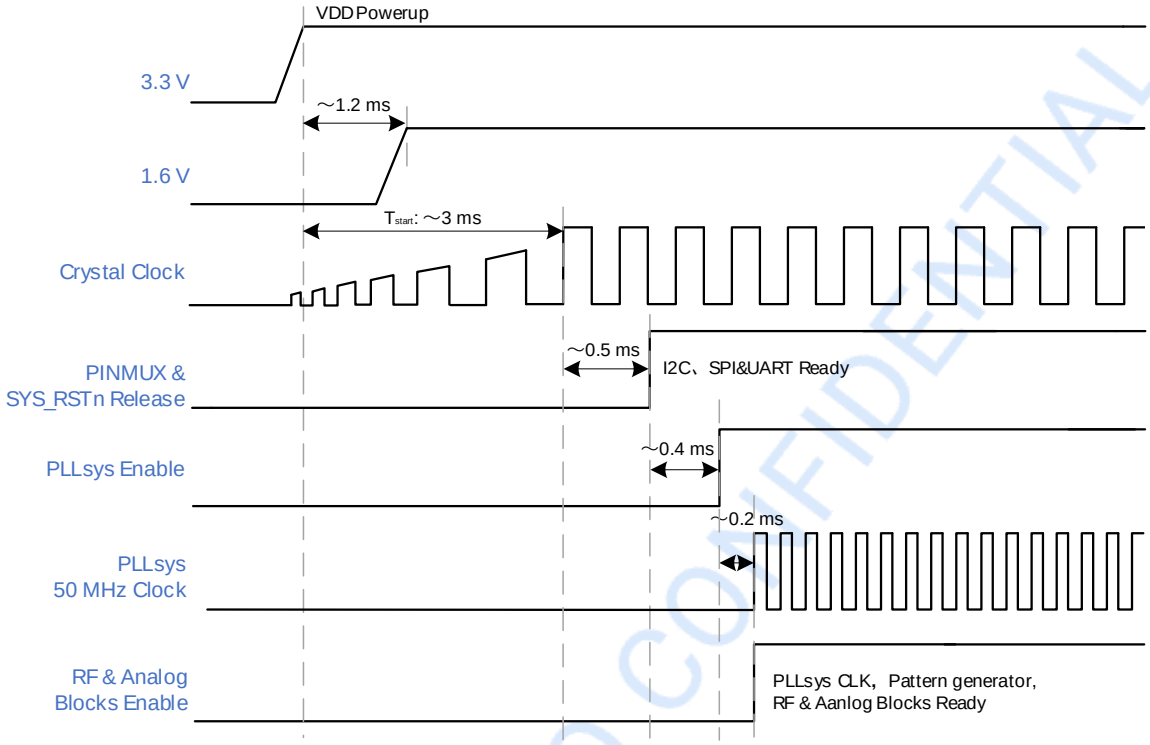


Figure 7-2 Power up timing and sequence

7.8.2 Hardware Reset Timing

The hardware reset requires an external reset pulse, as depicted in Figure 7-3. When the hardware reset is triggered, all internal registers of ICL111A will revert to their default values. Following the reset completion, it is imperative to re-configure all the chip's settings.

The hardware reset is activated when Pin RSTN is triggered by a logic low signal, and it is recommended to ensure that T_{RST} is greater than 2 ms.

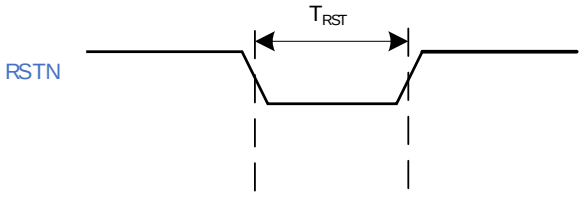


Figure 7-3 Reset pulse width

7.9 External Clock and Crystal Characteristics

The ICL111A necessitates an external clock source, either a 25 MHz crystal or an external clock input, for the initial boot and as a reference for the internal PLL within the device. Given that the feedback resistance is integrated on the chip, only a crystal and capacitors Ct1 and Ct2 need to be externally connected, specifically in the case of fundamental mode oscillation. The crystal implementation is illustrated in Figure 7-4.

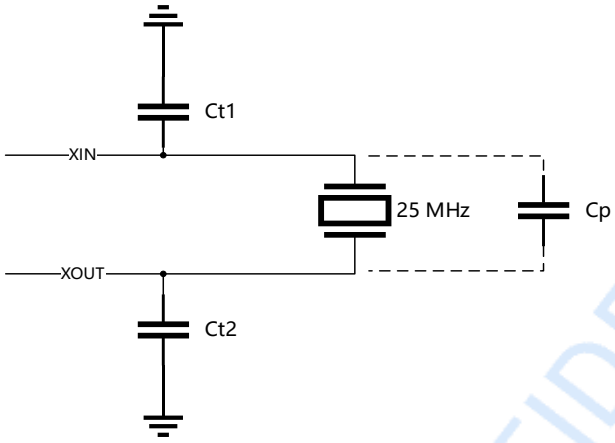


Figure 7-4 Crystal implementation

The load capacitors, Ct1 and Ct2, as depicted in Figure 7-4, should be selected to satisfy Equation 1. In this equation, C_L represents the load specified by the crystal manufacturer. It is crucial to place all discrete components utilized for the oscillator circuit as close as possible to the associated oscillator XIN and XOUT pins.

$$C_L = \frac{Ct1 \times Ct2}{Ct1+Ct2} + Cp \qquad \text{Equation 1}$$

Table 7-13 presents the electrical characteristics of the clock crystal.

Table 7-13 Crystal electrical characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
f_P	Parallel resonance crystal frequency	-	25	-	MHz
C_L[1]	Crystal load capacitance	5	10	20	pF
C_p	Crystal shunt capacitance	-	-	2	pF
ESR	Crystal ESR	-	-	50	Ω
Temperature range	Expected temperature range of operation	-40	-	85	°C
Frequency tolerance	Crystal frequency tolerance[1][2][3]	-50	-	50	ppm

Note:

[1] Should be adjusted in accordance with the load capacitance of the utilized crystal.

[2] The crystal manufacturer's specification must meet this requirement.

[3] This encompasses the initial tolerance of the crystal, drift over temperature, aging, and frequency pulling resulting from incorrect load capacitance.

[4] Crystal tolerance directly impacts radar sensor accuracy.

The clock signal becomes available when the crystal signal level stabilizes, usually around 3 ms after activating the supply lines to the ICL111A.

An external AC-coupled sine wave or DC-coupled square wave clock signal can serve as the reference clock for the ICL111A. The clock is input to the XIN pin only, and the XOUT pin should be left floating. The electrical characteristics of the external clock signal are shown in Table 7-14. To interface with o the XIN pin, the incoming clock signal should be AC-coupled using a 2-pF capacitor.

Table 7-14 External clock signal specifications

Parameter	Description	Min.	Typ.	Max.	Unit
fs	External clock signal frequency	-	25	-	MHz
Amp	AC clock signal amplitude	0.5	-	1.5	V(pp)
Duty cycle	Duty cycle of clock signal	-	50%	-	-
Frequency tolerance	Crystal frequency tolerance	-50	-	50	ppm
PN	Phase noise at 1 kHz	-	-	-135	dBc/Hz
	Phase noise at 100 kHz	-	-	-150	dBc/Hz
	Phase noise at 1 MHz	-	-	-150	dBc/Hz

8 Interface and Peripherals

The ICL111A features two types of digital communication interfaces: the chip configuration interface and the data output interface.

8.1 Chip Configuration Communication Interface

The configuration communication interface of the ICL111A is determined by the status of Pin H2 and Pin H3 during the power-up period. The ICL111A supports three types of configuration communication modes: I2C, SPI, and UART.

8.1.1 I2C for Configuration

The I2C module works as a slave terminator and encompasses the following features:

- The I2C interface adheres to the I2C-bus standard and utilizes open-drain pins;
- The I2C-bus interface supports Fast-mode with bit rate of up to 400 kHz;
- It facilitates bidirectional data communication between masters and slaves;
- The I2C module supports up to 4 I2C device addresses.

8.1.1.1 I2C Timing Characteristics

Table 8-1 I2C timing parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{scl}	SCL clock frequency	-	-	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	0.4	-	-	µs
t_{LOW}	Low time of the SCL clock	0.4	-	-	µs
t_{HIGH}	High time of the SCL clock	0.4	-	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	0.1	-	-	µs
$t_{HD;DAT}$	Data hold time	40	-	-	ns
$t_{SU;DAT}$	Data set-up time	50	-	-	ns
t_r	Rise time of both SDA and SCL signals	20	-	300	ns
t_f	Fall time of both SDA and SCL signals	20	-	300	ns
$t_{SU;STO}$	Set-up time for STOP conditions	0.1	-	-	µs
t_{BUF}	BUS free time between a STOP and START condition	1	-	-	µs

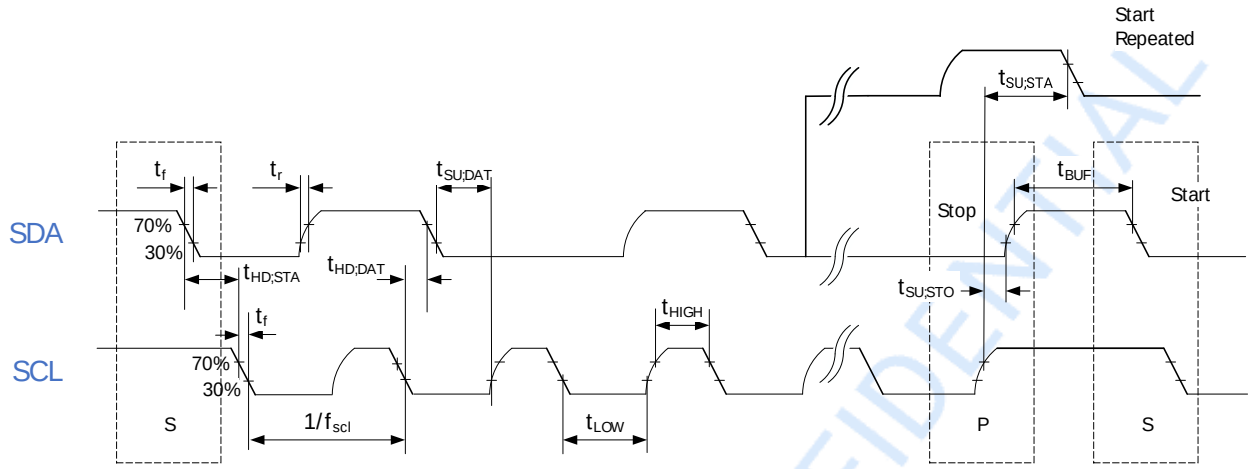


Figure 8-1 I2C timing diagram

The data on the SDA line must remain stable during the t_{HIGH} period, and can only undergo changes when the clock signal is low. Table 8-2 provides a list of acronyms used in I2C functionality.

Table 8-2 I2C abbreviations

Acronym	Description
SA[6:0]	The 7 bits slave address
SRA[7:0]	Slave Internal Register Address
DATA[x+7:x]	Data Word
R / $\overline{W}$	Read/Write (0 = data from master to slave, 1 = data from slave to master)
ACK	Acknowledgement
NACK	Non-Acknowledgement (=1)
S	Start condition (initiated by the master)
Sr	Repeated Start condition (initiated by the master)
P	Stop condition (initiated by the master)

8.1.1.2 I2C Interface Data Protocol

The ICL111A Configuration_I2C interface operates in a byte data format. The generation of Start and Stop conditions is the responsibility of the external master terminator, and is represented by the S and P parts in Figure 8-2. The first byte following the Start condition comprises a 7-bit slave address followed by the R / $\overline{W}$ bit.

When R / $\overline{W}$ = 0, the master writes data to the addressed slave.

When R / $\overline{W}$ = 1, the master reads data from the slave.

An additional clock cycle dedicated to acknowledgement (ACK) follows each byte. If the slave inserts an ACK after the first byte from the master, it is followed by 8 bits of data from the transmitter (either master or slave, depending on the R / $\overline{W}$ bit). After receiving the data bits, the receiver appends an ACK bit.

To disregard the readback message, the master terminator must transmit a no-acknowledge (NACK) bit during the acknowledge clock cycle on the bus.

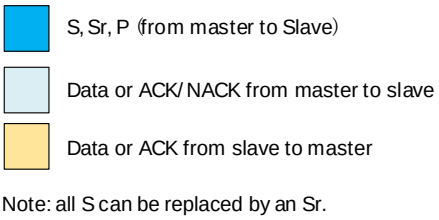


Figure 8-2 I2C color conventions

8.1.1.3 I2C Write

A typical I2C write operation for chip configuration is illustrated in Figure 8-3.

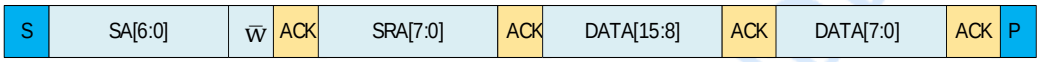


Figure 8-3 I2C configuration communication Write

8.1.1.4 I2C Read

In a read sequence (bit R / $\overline{W}$ = 1), the master provides an acknowledgement (ACK) after each data byte. After the last data byte, the master responds with a non-acknowledgement (NACK). A typical I2C read operation for chip configuration is illustrated in Figure 8-4.

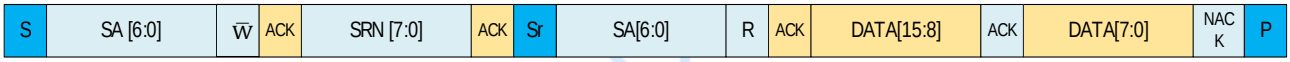


Figure 8-4 I2C configuration communication Read

8.1.2 SPI for Configuration

The ICL111A chip configuration SPI supports full-duplex communication and offers the following features:

- Maximum SPI speed of 3.125 MHz;
- Synchronous serial communication;
- Operation in slave mode with mode00 configuration.

8.1.2.1 Configuration SPI Interface Timing Characteristic

Table 8-3 Configuration SPI timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
$T_{c(sclk)}$	Clock period	320	-	-	ns
T_{sclk_high}	Clock high time	160	-	-	ns
T_{sclk_low}	Clock low time	160	-	-	ns
$T_{h(CSN)}$	Chip select hold time	320	-	-	ns
$T_{su(SI)}$	SPI MOSI input setup time	40	-	-	ns
$T_{h(SI)}$	SPI MOSI input data hold time	40	-	-	ns
$T_{a(SO)}$	SPI data output access time	0	-	-	ns
$T_{h(SO)}$	SPI data output hold time	40	-	-	ns
$T_{v(SO)}$	SPI MOSI data output valid time	-	-	120	ns
T_{cs_sclk}	SPI CSN setup time	160	-	-	ns

T_{sclk_cs}	SPI CSN hold time	160	-	-	ns
T_{cs_cs}	SPI CSN disable to next CSN enable time	320	-	-	ns
POL_{clk}	SPI clock polarity (CPOL)	-	0	-	-
ϕ_{clk}	SPI clock phase (CPHA)	-	0	-	-

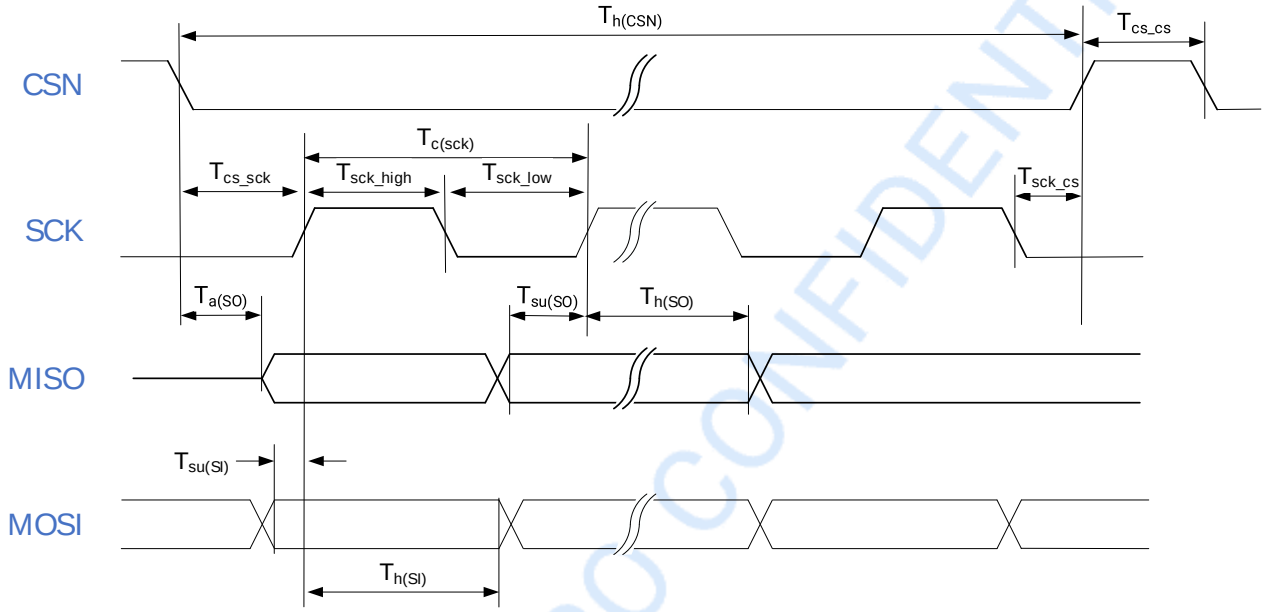


Figure 8-5 Configuration SPI interface timing diagram

8.1.2.2 Configuration SPI Interface Data Protocol

The ICL111A configuration SPI interface operates in 4-wire communication mode, controlling the system through a single SPI protocol handler that interfaces with multiple register interfaces within each sub-block.

The pin nomenclature for interfacing with a host MCU is as follows: “SCLK” serves as the serial clock input, operating at a maximum bus signaling rate of 3.125 MHz; “MOSI” (Master Out Slave In) functions as the serial input for writing data into the ICL111A; “MISO” (Master In Slave Out) serves as the serial output for reading data from the ICL111A; and “CSN” (Chip Select) is the select pin used for both write and read operations.

The ICL111A SPI operates in a byte data format. The data frame begins with the R / $\overline{W}$ bit, followed by 7 bits A0~A6. In the communication process, 2 bytes of data will be read or written.

When R / $\overline{W}$ = 0, the master writes data to the addressed slave.

When R / $\overline{W}$ = 1, the master reads data from the slave.

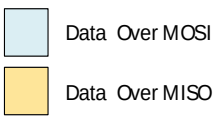


Figure 8-6 SPI color conventions

8.1.2.3 SPI Write

The SPI interface is used to write data into a single 16-bit register. A typical SPI write operation for chip configuration data is depicted in Figure 8-7. The write operation begins with the R / $\overline{W}$ bit, followed by the register address (7 bits), and concludes with a payload message of 16 bits.

Figure 8-7 SPI configuration Write

8.1.2.4 SPI Read

The timing for the MISO interface is shown in Figure 8-8. The provided interface protocol is applicable only when the first bit of MOSI (R / $\bar{W}$ bit) is set to '1'.

Figure 8-8 SPI configuration Read

8.1.3 UART for Configuration

The ICL111A chip configuration UART interface features both TX and RX lanes, with a typical data communication speed at 115200 bps.

8.1.3.1 Configuration UART Interface Timing Characteristic

Table 8-4 Configuration UART interface timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
Bd	Baud Rate	-	115200	-	bps

8.1.3.2 Configuration UART Interface Data Protocol

The ICL111A configuration SPI interface is structured around a combination of a single UART protocol handler and several register interfaces within each sub-block.

For interfacing with a host controller, the pin nomenclature is as follows: "Configuration_UART_RX" serves as the serial input for writing data into the ICL111A, while "Configuration_UART_TX" functions as the serial output for reading data from the ICL111A.

The ICL111A UART interface operates in asynchronous communication mode and does not require a clock pin. The data frame initiates with a start bit ('0'), followed by an 8-bit data payload with an additional parity bit, and ends with one stop bit.

During UART configuration operations, data sent to the ICL111A should include one parity bit, and the ICL111A does not verify the parity. Data sent from the ICL111A includes an additional 1-bit odd parity.

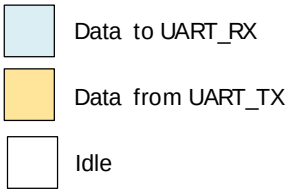


Figure 8-9 UART color conventions

8.1.3.3 Configuration UART Write

The UART interface is used for writing into a single 16-bit register. A typical UART chip configuration is

illustrated in Figure 8-10. The configuration operation command comprises three sections: the first section transmits the 7-bit slave address and 1-bit R / $\overline{W}$; the subsequent two sections write the data values to the slave address. The payload message, consisting of 16-bit data, is divided into two sections (low bits and high bits). These sections adhere to the format of starting with a start bit (‘0’), followed by 8 bits data, concluding with a parity check bit and a stop bit.

The data Write or Read enable bit located in the slave address section.

When R / $\overline{W}$ = 0, the master writes data to the addressed slave.

When R / $\overline{W}$ = 1, the master reads data from the slave.

Abbreviations:

S: Start bit.

SRA: Slave internal register address.

PA: Parity check bit.

P: Stop bit.

I: Idle bits.

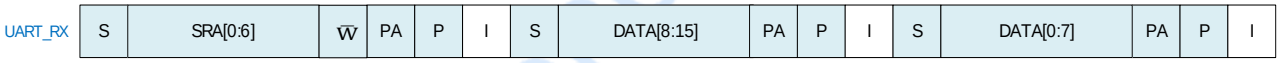


Figure 8-10 UART configuration Write

8.1.3.4 Configuration UART Read

The timing of the Read operation is illustrated in Figure 8-11. The provided interface protocol is applicable only when the first bit of UART_RX (R / $\overline{W}$ bit) is set to ‘R’.

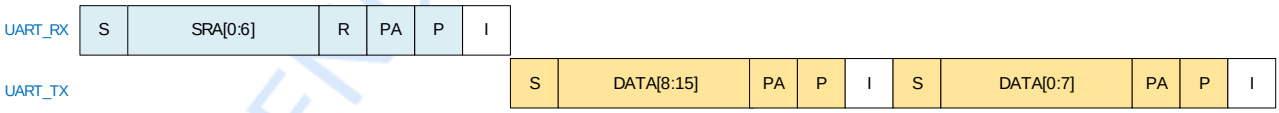


Figure 8-11 UART configuration Read

8.2 Chip Data Communication Interface

The data communication mode for the ICL111A is determined by the register settings. The ICL111A supports two types of data communication modes: SPI and UART. Both SPI and UART interfaces transmit the DS RAW/DSP processed data to the receiver.

8.2.1 SPI for Data Communication

The ICL111A chip’s data communication SPI interface is versatile and can operate in both master mode and slave mode. By default, Pin H6 “SPI_DO” (MOSI) transmits RX’s data. The configuration for master mode or slave mode is adjustable through register settings.

The SPI interface supports data output with DS RAW / frames of FFT data flowing from the master to the slave. It includes the following features:

- Maximum SPI speed of 25 MHz in master mode;
- Maximum SPI speed of 7 MHz in slave mode;
- Operation in Mode00.

8.2.1.1 SPI Interface Timing Characteristic

Table 8-5 Data Communication SPI timing characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$T_{c(sclk)}$	Clock period	Master mode	40	-	2560	ns
		Slave mode	140	-	-	ns
T_{sclk_high}	Clock high time	Master mode	13	-	-	ns
		Slave mode	70	-	-	ns
T_{sclk_low}	Clock low time	Master mode	27	-	-	ns
		Slave mode	70	-	-	ns
$T_{\_h(MO)}$	SPI data output hold time	Master mode	0	-	-	ns
$T_{\_h(SO)}$		Slave mode	40	-	-	ns
$T_{\_v(MO)}$	SPI DO data output valid time	Master mode	15	-	-	ns
$T_{\_v(SO)}$		Slave mode	-	-	70	ns
$T_{\_a(SO)}$	Data output access time	Slave mode	0	-	-	ns
T_{cs_scl}	SPI CSN setup time	Master mode	60	-	-	ns
		Slave mode	70	-	-	ns
T_{scl_cs}	SPI CSN hold time	Master mode	40	-	-	ns
		Slave mode	70	-	-	ns
T_{cs_cs}	SPI CSN disable to next CSN enable time	Master mode	120	-	-	ns
		Slave mode	210	-	-	ns
T_{rdy}	Data is ready for transmission	Slave mode	0	-	-	-
POL_{clk}	SPI clock polarity (CPOL)	Master mode Slave mode	-	0	-	-
ϕ_{clk}	SPI clock phase (CPHA)	Master mode Slave mode	-	0	-	-

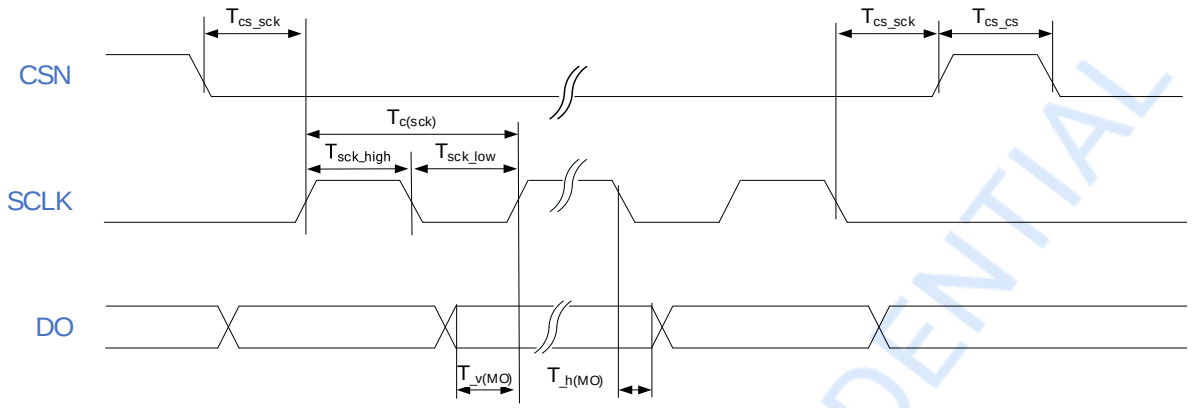


Figure 8-12 Data communication SPI timing diagram – master mode

In slave mode, Pin H4 will transmit a logic “1” to indicate that data output is ready. When DO data is prepared for transmission at Pin H6, the external master will send CSN and SCLK signals to the ICL111A’s Pin H5 and Pin G8. Following this, the data can be output in accordance with the SPI slave mode timing shown in Figure 8-13. After the transmission of the last bit of data, the external SCK signal transitions to logic “0”, and the external CSN shifts to logic “1” based on the data length.

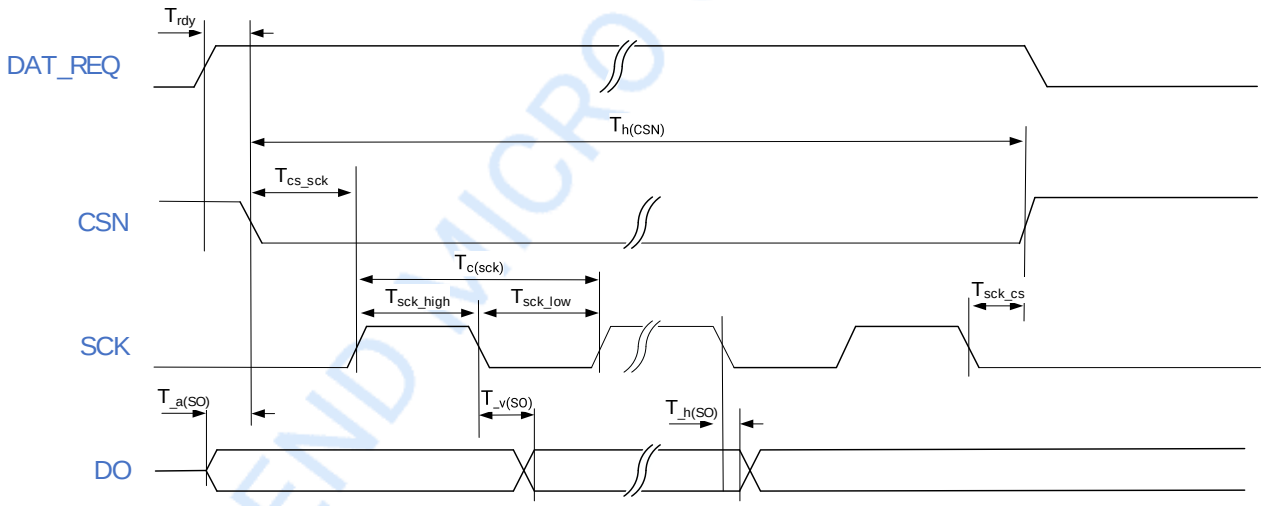


Figure 8-13 Data communication SPI timing diagram - slave mode

During the chip configuration period, the data output from SPI is not guaranteed. All data transmitted through the DATA_SPI channel follow the format shown in Figure 8-14.

Figure 8-14 DATA channel transmission

8.2.1.2 SPI Output for Range FFT

When the Range FFT data SPI output mode is selected through the chip configuration command, the chip will transmit Range FFT data. The pin nomenclature for interfacing is as follows: Pin G8 “SPI_SCLK” serves as the serial clock output; Pin H6 “SPI_DO” is RX port’s serial data from the ICL111A; and Pin H5 “SPI_CSN” (Chip Select) is the select pin for read operations.

Interface and Peripherals

The ICL111A data communication SPI operates in a 32-bit format. The data frame initiates with the header Dword (32 bits); subsequently, all the FFT data is sent out. The high 16 bits represent real part of the FFT data, and the low 16 bits represent imaginary part of the FFT data. Finally, the tail Dword (32 bits) validates the check_sum and terminates the data output.

The data output is in MSB first order, and the Range FFT data type is signed integer. Table 8-6 illustrates the Range FFT data format over DO.

Table 8-6 Range FFT data frame format over DO

Header[Dword 0]	'b1010 1010	'b 0	'b 011	FFT_chirp_index1 (bit 7:0, 8)[19:11][1]	CFG_FFT_TX_MAX[10:0][2]			
Data[Dword 1]	FFT real data 0[31:16]				FFT Imaginary data 0[15:0]			
Data[Dword 2]	FFT real data 1[31:16]				FFT Imaginary data 1[15:0]			
Data[Dword …]	FFT real data …[31:16]				FFT Imaginary data …[15:0]			
Data[Dword m]	FFT real data m-1[31:16]				FFT Imaginary data m-1[15:0]			
Tail[Dword m+1]	Check_sum[31:16][3]				FFT_FRAME_INDEX [15:12][4]	'b 00 [5]	CFG_MSG [9:8][6]	'b 0101 0101

Note:

[1] FFT_chirp_index1(bit 7:0, 8)[19:11]: Represents the chirp sequence number in one frame, starting from “0” in each frame. The most significant bit (MSB) is located at bit 11, and bits 19:12 range from MSB-1 to least significant bit (LSB).

[2] CFG_FFT_TX_MAX[10:0]: Denotes the number of m (the total FFT output points) +1 in this chirp.

[3] Check_sum[31:16]: Signifies the sum of all data in this chirp, equal to the value of the low 16 bits of the sum result.

[4] FFT_FRAME_INDEX[15:12]:Indicates the frame num counter, starting from 0.

[5] Default value is 0 and can act as frame_cnt[1:0] with extra configuration.

[6] CFG_MSG[9:8]: Represents user-defined bits.

8.2.1.3 SPI Output for Doppler FFT

When the Doppler FFT data SPI output mode is selected through the chip configuration command, the chip will output Doppler FFT data. The pin nomenclature for interfacing is as follows: Pin G8 “SPI_SCLK” serves as the serial clock output; Pin H6 “SPI_DO” is RX port’s serial data from the ICL111A; and Pin H5 “SPI_CSN” (Chip Select) is the select pin for read operations.

The ICL111A data communication SPI operates in a 32-bits format. The data frame begins with the header Dword (32 bits). Subsequently, all the Doppler FFT data is sent out, with the high 16 bits representing the real part of the Doppler FFT data, and the low 16 bits representing the imaginary part. Finally, the tail Dword (32 bits) validates the check_sum and terminates the data output.

The data output is in MSB first order, and the Doppler FFT data type is signed integer. Table 8-7 illustrates the Doppler FFT data format over DO.

Table 8-7 Doppler FFT data frame format over DO

Header[Dword 0]	'b1010 1010	'b 0	'b 100	DFFT_chirp_index1(bit 7:0, 8) [19:11][1]		DW_LEN[10:0][2]	
Data[Dword 1]	DFFT real data 0[31:16]			DFFT imaginary data 0[15:0]			
Data[Dword 2]	DFFT real data 1[31:16]			DFFT imaginary data 1[15:0]			
Data[Dword …]	DFFT real data …[31:16]			DFFT Imaginary data …[15:0]			
Data[Dword m]	DFFT real data m-1[31:16]			DFFT Imaginary data m-1[15:0]			
Tail[Dword m+1]	Check_sum[31:16][3]			FFT_FRAME_INDEX [15:12][4]	'b 00	CFG_MSG[9:8] [5]	'b 0101 0101

Note:

[1] DFFT_chirp_index1(bit 7:0, 8)[19:11]: Represents the chirp sequence number in one frame, starting from “0” in each frame. The most significant bit (MSB) is located at bit 11, and bits 19:12 range from MSB-1 to least significant bit (LSB).

[2] DW_LEN[10:0]: Indicates the Doppler FFT data num counter, starting from 0.

[3] Check_sum[31:16]: Signifies the sum of Doppler FFT data in this frame, equal to the value of the low 16 bits of the sum result.

[4] FFT_FRAME_INDEX[15:12]: Indicates the frame num counter, starting from 0.

[5] CFG_MSG[9:8]: Represents user-defined bits.

8.2.1.4 SPI Output for DS RAW

When the DS RAW data SPI output mode is selected through the chip configuration command, the chip will output DS RAW data. The pin nomenclature for interfacing is as follows: Pin G8 "SPI_SCLK" serves as the serial clock output; Pin H6 "SPI_DO" is the RX's serial data from the ICL111A; and Pin H5 "SPI_CSN" (Chip Select) is the select pin for read operations.

The ICL111A can output down-sampled RAW data (downsampling rates: 1/2, 1/4, 1/8). DS RAW data communication SPI operates in a 32-bit format. The data frame initiates with the header Dwords; subsequently, all the DS RAW data is sent out. The high 16 bits represent the real part of the DS RAW data, and the low 16 bits represent the imaginary part. Finally, the tail Dwords validate the check_sum and terminate the data output.

The data output is in MSB first order, and the DS RAW data type is signed integer. Table 8-8 illustrates the DS RAW data format over DO.

Table 8-8 DS RAW data frame format over DO

Header[Dword 0]	‘b1010 1010	‘b 0	‘b 010	RAW_chirp_cnt (bit 7:0, 8) [19:11][1]		RAW_DATA_cnt[10:0][2]	
Data[Dword 1]	DS RAW real data 0[31:16]			DS RAW Imaginary data 0[15:0]			
Data[Dword 2]	DS RAW real data 1[31:16]			DS RAW Imaginary data 1[15:0]			
Data[Dword …]	DS RAW real data …[31:16]			DS RAW Imaginary data …[15:0]			
Data[Dword m]	DS RAW real data m-1[31:16]			DS RAW Imaginary data m-1[15:0]			
Tail[Dword m+1]	Check_sum[31:16][3]			RAW_FRAME_INDEX [15:12]	'b 00	CFG_MSG [9:8][5]	'b 0101 0101

Note:

[1] RAW_chirp_cnt (bit 7:0, 8)[19:11]: Represents the chirp sequence number in one frame, starting from "0" in each frame. The most significant bit (MSB) is located at Frame data's bit 11, and bits 19:12 range from MSB-1 to least significant bit (LSB).

[2] RAW_DATA_cnt[10:0]: Denotes the number of m (the total items of DS RAW data) in this chirp.

[3] Check_sum[31:16]: Signifies the sum of all data in this frame, equal to the value of the low 16 bits of the sum result.

[4] RAW_FRAME_INDEX[15:12]: Represents the chirp sequence number in one frame, it equals RAW_chirp_cnt[19:11]'s low 4 bits value.

[5] CFG_MSG[9:8]: Denotes user-defined bits.

8.2.1.5 SPI Output for CFAR Report

The ICL111A can transmit CFAR Report data via SPI, using Pin H6 as the data output bus. The data output is in MSB first order, and the CFAR Report data type is signed integer.

Table 8-9 CFAR Report frame format

Header[Dword 0]	'b1010 1010	'b1	'b 000	'b 0 0000 0000	CFG_LEN_RPT[10:0][1]	
Data[Dword 1]	'b 0 0000 0000		CFAR_PMAX3_didx[22:16][2]	'b 0 0000 0000	CFAR_PMAX3_ridx[6:0][3]	
Data[Dword 2]	CFAR_PMAX3_value[31:0][4]					
Data[Dword 3]	'b 0 0000 0000		CFAR_PMAX2_didx[22:16]	'b 0 0000 0000	CFAR_PMAX2_ridx[6:0]	
Data[Dword 4]	CFAR_PMAX2_value[31:0]					
Data[Dword 5]	'b 0 0000 0000		CFAR_PMAX1_didx[22:16]	'b 0 0000 0000	CFAR_PMAX1_ridx[6:0]	
Data[Dword 6]	CFAR_PMAX1_value[31:0]					
Data[Dword 7]	'b 0 0000 0000		CFAR_PMAX0_didx[22:16]	'b 0 0000 0000	CFAR_PMAX0_ridx[6:0]	
Data[Dword 8]	CFAR_PMAX0_value[31:0]					
TAIL[Dword 9]	Check_sum[31:16][5]			DPL_frame_cnt[15:12][6]	'b 00	CFG_MSG[9:8][7]	'b 0101 0101

Note:

[1] CFG_LEN_RPT[10:0]: Denotes the length of Data payload; the maximum value is 27.

[2] CFAR_PMAXm_didx[22:16]: Represents Doppler FFT CFAR location, Doppler FFT index; PMAXm ranges from PMAX3 to PMAX0, and is related to the 4 subdivided detect zones.

[3] CFAR_PMAXm_ridx[6:0]: Indicates Doppler FFT CFAR location, Range FFT index; PMAXm ranges from PMAX3 to PMAX0, and is related to the 4 subdivided detect zones.

[4] CFAR_PMAXm_value[31:0]: Specifies Doppler FFT CFAR value; PMAXm ranges from PMAX3 to PMAX0, and is related to the 4 subdivided detect zones.

[5] Check_sum[31:16]: Signifies the sum of all data in this frame, equal to the value of the low 16 bits of the sum result.

[6] DPL_frame_cnt[15:12]: Represents the Doppler frame num counter, starting from 0.

[7] CFG_MSG[9:8]: Represents user-defined bits.

8.2.2 UART Output for Data Communication

The ICL111A data communication UART interface only includes the TX lane, and its electrical characteristics are listed in Table 8-10.

Table 8-10 Data communication UART interface electrical characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Bd	Baud Rate	4800	-	256000	bps

The ICL111A DATA_UART_TX interface can also output in Data SPI mode, including DATA_SPI_DO's data, such as Range FFT data, Doppler FFT data, and CFAR reports. DATA_UART_TX transmits the data with an odd parity bit. The format is organized from the highest byte of DW0 to the lowest byte, then goes to the next DW, continuing until the last DW(DWx). Each byte is transmitted from LSB to MSB.

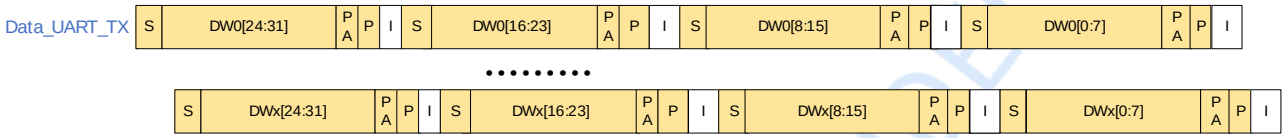
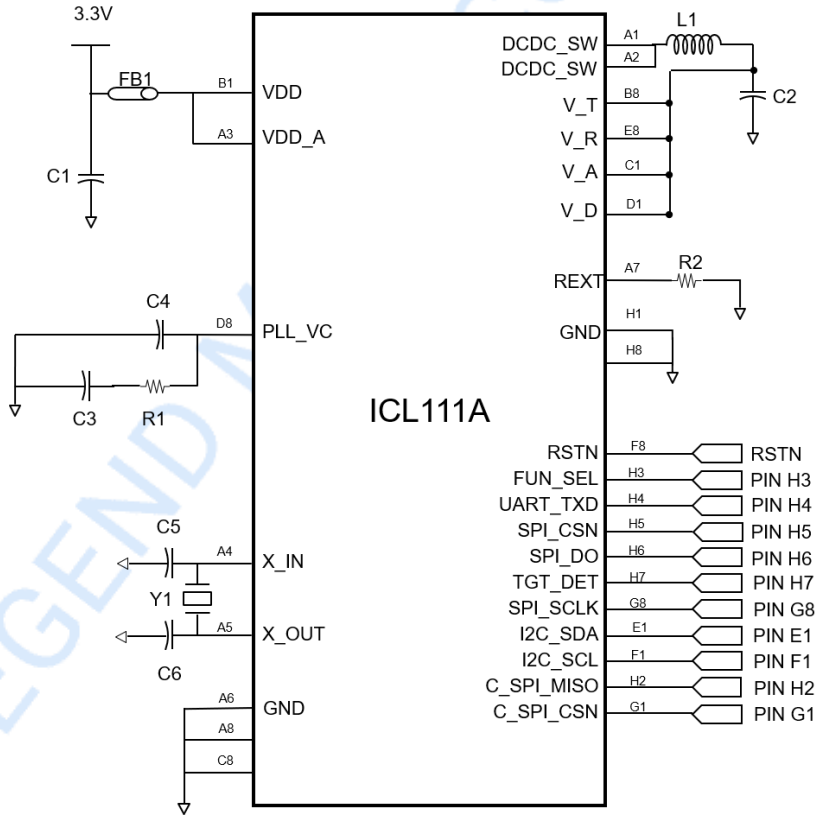


Figure 8-15 UART output data timing

9 Application Information



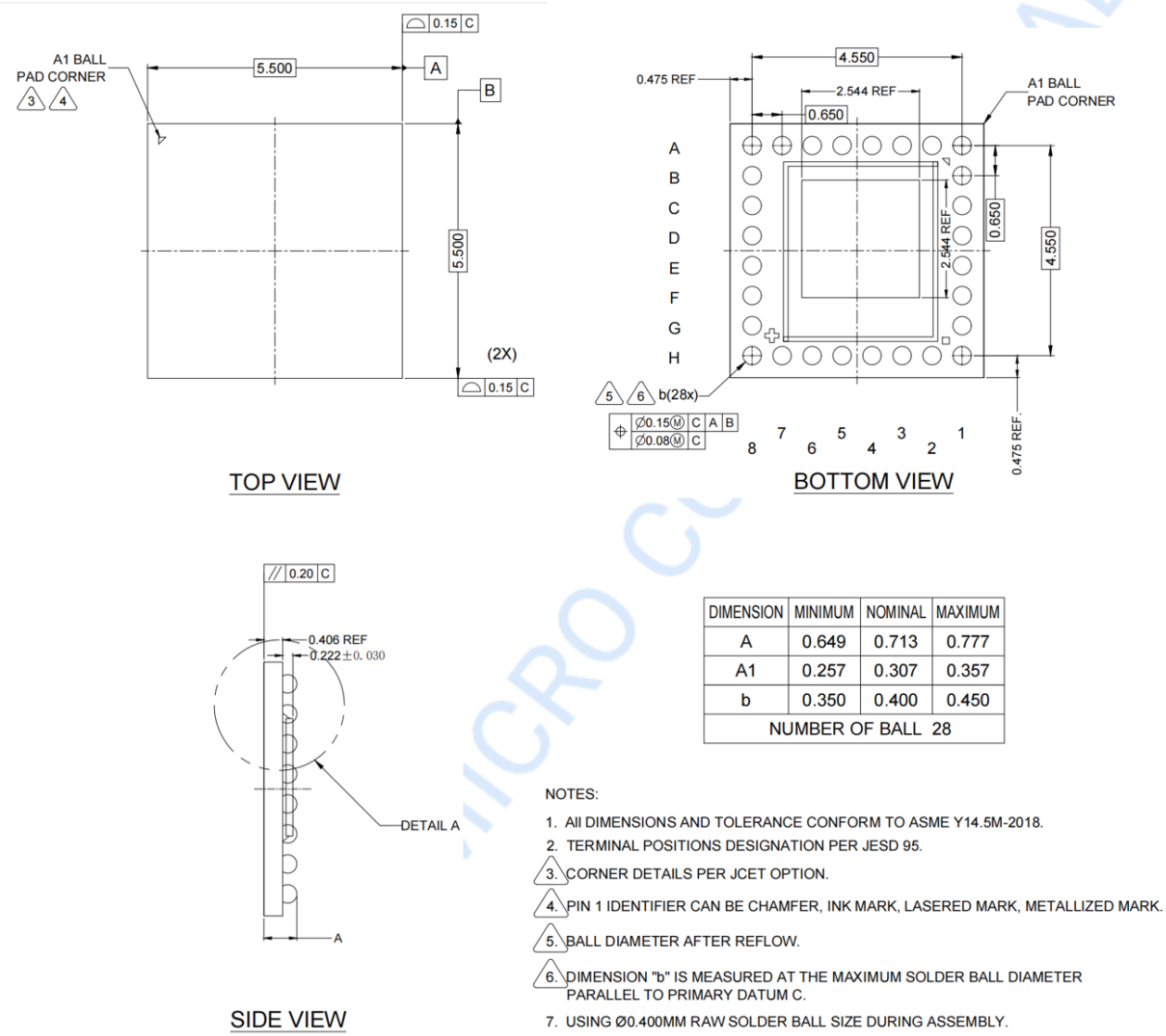
Application Information

Figure 9-1 ICL111A application schematic

Table 9-1 External component suggestions

Component	Description	Value	Remarks
FB1	ferrite bead	GZ1005D310TF	-
C1	ceramic capacitor	100 nF	X7R
C2	DCDC output ceramic capacitor	22 μF	X5R
L1	DCDC output power inductor	22 μH	XRCD32-220K, ±10%, DCR < 0.5Ω, Isat > 500 mA
R1	loop filter resistor	1.6 kΩ	±5%
C3	loop filter ceramic capacitor	2.7 nF	±5%, X7R
C4	loop filter ceramic capacitor	390 pF	±5%, X7R
R2	resistor	12.4 kΩ	±1%
C5, C6	capacitor	12 pF	±5%, C0G
Y1	crystal	25 MHz	<50 ppm

10 Package Outline



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.649	0.713	0.777
A1	0.257	0.307	0.357
b	0.350	0.400	0.450
NUMBER OF BALL 28			

NOTES:

1. All DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2018.
2. TERMINAL POSITIONS DESIGNATION PER JESD 95.
3. CORNER DETAILS PER JCET OPTION.
4. PIN 1 IDENTIFIER CAN BE CHAMFER, INK MARK, LASERED MARK, METALLIZED MARK.
5. BALL DIAMETER AFTER REFLOW.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
7. USING Ø0.400MM RAW SOLDER BALL SIZE DURING ASSEMBLY.

Figure 10-1 Package description

11 Handling Information

ESD CAUTION

ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

12 Revision History

Revision	Date	Data Sheet Status	Contents
0.1	2022/11/5	Objective Data Sheet	Initial draft.
0.2	2024/12/6	Objective Data Sheet	Updated pin diagram, pin description table, application schematics, and package outline; Unified table and note formats; Updated low power and power control descriptions in Main Features; Added 5.3.2 Standalone Mode_Auto_Mode section; Added Trigger Delay and Absence Report Delay to Table 5-3; Updated data in Table 7-1 and Table 7-8, modified parameter names and descriptions in Table 7-11.

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