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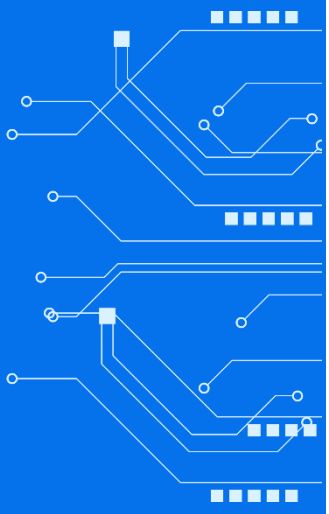
Product Data Sheet

Rev.1.1 2023/9/9

ICL1112

Smart mmWave Sensor Series



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ICL1112

1 General Description

The ICL1112 is an integrated single-chip mmWave sensor SoC based on FMCW radar transceiver technology. It works in the 24 GHz K-band with up to 1 GHz modulation bandwidth in each single frequency sweeping chirp.

The ICL1112 offers a fully integrated solution for all critical mmWave functions with full transceiver and signal processing path, including full K-band RF transceiver, on-chip pattern generator, PLL, and ADCs. The pattern generator supports multiple frequency sweeping modes with different time-frequency waveforms, e.g. saw-tooth and triangular waveforms. The pattern generator and PLL support fast chirp mode up to 8 kHz chirp rate. The digitized signals from the receiver chain can be serialized via multiple output interfaces.

The device is packaged in a 32 pin 4 mm × 4 mm leadless ROHS compliant QFN package for easy interfacing to a wide range of antenna board technologies.

2 Main Features

- 24 GHz K-band highly integrated FMCW radar sensor SoC
- Up to 1 GHz bandwidth FM tuning range
- Integrated signal generator, low phase noise PLL, transmitter, receiver, baseband and ADCs
- One transmit channel and one receive channel
- Ultra-low power: As low as 55 μA current dissipation with 0.3% duty cycle operation
- TX maximum output power: 12 dBm
- RX noise figure: 10.0 dB
- Phase noise @ 1 MHz offset: -97 dBc/Hz
- Built-in 2.5 MHz conversion rate ADC with 16 bits resolution
- Fast FMCW chirp ramp rate: up to 20 MHz/μs
- High FMCW chirp linearity of 0.45‰ at 250 MHz tuning range
- Precise TX power control enhanced by on-chip power detector and temperature sensor
- Built-in hardware accelerator, support complex FFT and CFAR function
- Configuration interface support: I2C/SPI/UART
- Data output interface support: DS RAW/SPI (master/slave mode)/UART
- Support flexible power supply modes
- Easy hardware design: 4 mm × 4 mm QFN32 package for ultra-compact PCB design
- Junction temperature range: –40°C to 105°C

3 Applications

- Smart Home Radar Sensor
- Smart Lock / Ring Bell
- Proximity and Position Sensor
- Home Appliance Radar Sensor
- Motion Detector
- Gesture Recognition

Table of Contents

1 General Description 1
2 Main Features 1
3 Applications 1
4 Block Diagram 3
5 Terminal Configuration and Description 4
5.1 Pin Diagram 4
5.2 Signal Descriptions 4
5.3 Pin Mux function 5
5.4 Standby Mode 6
5.5 Chip Configuration Pin States Configuration 6
6 Functional Description 7
6.1 Transceiver Section 7
6.2 Waveform Generator Section 7
6.3 DSP Accelerator 8
6.4 CFAR Function 9
6.5 Power Supply Section 9
6.6 Temperature Sensor 10
6.7 Power detector 10
7 Electrical Characteristics 10
7.1 Absolute Maximum Ratings 10
7.2 ESD Ratings 11
7.3 Thermal Resistance 11
7.4 Recommended Operating Conditions 11
7.5 Power Supply Characteristics 11
7.6 Dynamic Performance 12
7.7 Timing and Switching Characteristics 14
7.8 External Clock and Crystal Characteristics 15
8 Interface and Peripherals 16
8.1 Chip Configuration Communication Interface 16
8.2 Chip Data Communication Interface 22
9 Application Information 28
9.1 Application Schematic 28
10 Package Outline 29
11 Handling Information 30
12 Revision History 30
Important Notice and Warnings 31

4 Block Diagram

The RF and analog subsystem implements the FMCW (frequency-modulated continuous-wave) transceiver system with one transmitter (TX), one receiver, synthesizer, mixer, and baseband. Gain controls are applied to both transmitter and receiver to adjust the whole link budget to work in different scenarios. The baseband includes inter-mediate frequency (IF) programmable amplifier, filters, and ADCs. A built-in DSP accelerator can process the IQ ADC's raw data with Range FFT or Doppler FFT.

The ICL1112 can be configured via I2C/SPI/UART interface, DS RAW data can be directly outputted, DSP processed data can be serialized and outputted via SPI/UART interface.

Figure 4-1 presents the illustration of the design of ICL1112.

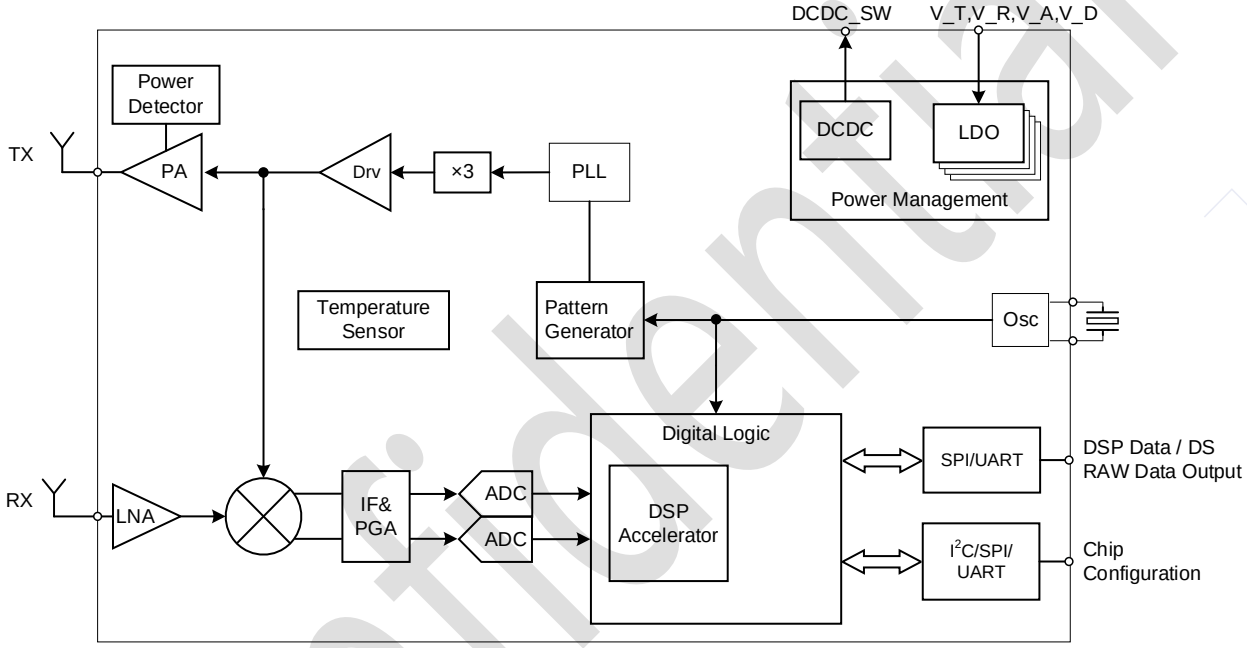


Figure 4-1 ICL1112 block diagram

5 Terminal Configuration and Description

5.1 Pin Diagram

The outlook of ICL1112 is shown in Figure 5-1.

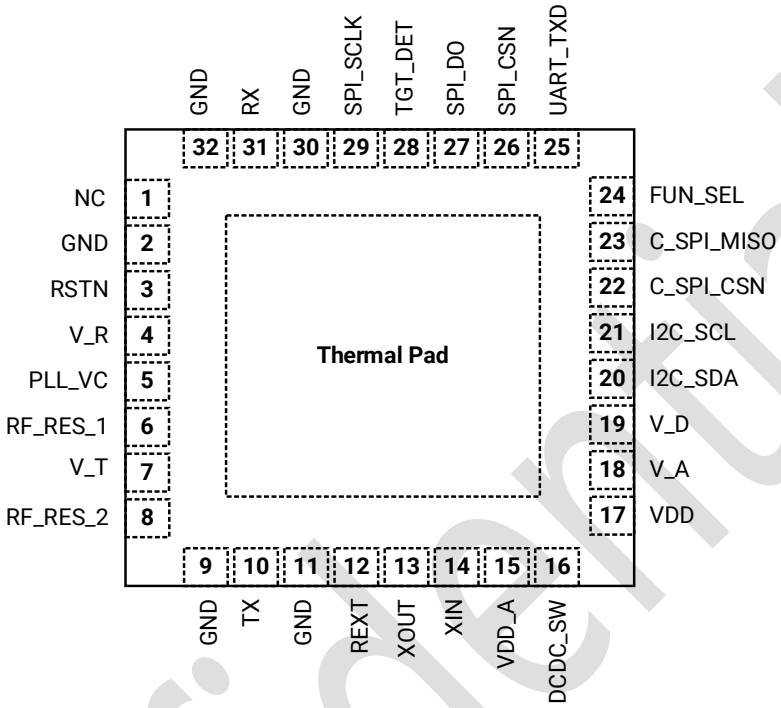


Figure 5-1 Pin diagram QFN32 (top view)

5.2 Signal Descriptions

Information of each pin is given in Table 5-1.

Table 5-1 Pin descriptions

Pin Name	Ball_No	Type	Description
NC	1	NC	No electrical connection internally. It may be left floating or connected to ground
RSTN	3	IN	External hardware reset input: A logic LOW on this pin resets the device, causing internal digital circuit to take their default states
V_R	4	Power	1.6 V analog power supply for RX sections
PLL_VC	5	IN	Connected to external loop filter to drive the internal VCO
RF_RES_1	6	OUT	Reserved RF pin, connect to Pin 8
V_T	7	Power	1.6 V analog power supply for TX sections
RF_RES_2	8	IN	Reserved RF pin, connect to Pin 6
TX	10	OUT	Single-ended transmitter output port

REXT	12	IN	Current bias circuit input, connect to ground with a bias resistor
XOUT	13	OUT	Crystal oscillator Output port
XIN	14	IN	Crystal oscillator or external clock Input port
VDD_A	15	Power	3.3 V power supply for analog domain
DCDC_SW	16	OUT	DCDC regulator switch node. Connect to the power inductor
VDD	17	Power	3.3 V power supply for the DCDC converter and digital domain
V_A	18	Power	1.6 V power supply for analog circuits
V_D	19	Power	1.6 V power supply for digital circuits
I2C_SDA	20[1]	OD	Configuration_I2C_SDA: Configuration channel I2C data I/O (open drain)
		IN	Configuration_SPI_MOSI: Configuration channel SPI data input
		IN	Configuration_UART_RX: Configuration channel UART receiver
I2C_SCL	21[1]	IN	Configuration_I2C_SCL: Configuration channel I2C clock
		IN	Configuration_SPI_SCLK: Configuration channel SPI serial clock
		OUT	Configuration_UART_TX: Configuration channel UART transmitter
C_SPI_CSN	22	IN	Configuration_SPI_CSN: Configuration channel SPI chip select enable
C_SPI_MISO	23[1]	OUT	Configuration_SPI_MISO: Configuration channel SPI data output
		IN	Chip pin mux function, see Table 5-2
FUN_SEL	24	IN	Chip pin mux function, see Table 5-2
UART_TXD	25[1]	IN	Standby mode pin mux function (internally pull down), see Table 5-4
		OUT	DAT_REQ: Data Channel data ready indication at SPI Slave mode
		OUT	DATA_UART_TX: Data channel UART output
SPI_CSN	26[1]	OUT/IN	DATA_SPI_CSN: DATA channel SPI chip select enable
		OUT	GPIO Output, Zone Detect 3. High: target exists; Low: No target
SPI_DO	27[1]	IN	Configuration channel I2C address high bit configuration, see Table 5-3
		OUT	DATA_SPI_DO: DATA channel SPI data output at RX channel
		OUT	GPIO Output, Zone Detect 0. High: target exists; Low: No target
TGT_DET	28[1]	IN	Configuration channel I2C address low bit configuration, see Table 5-3
		OUT	GPIO Output, Zone Detect 1. High: target exists; Low: No target
SPI_SCLK	29[1]	OUT/IN	DATA_SPI_SCLK: DATA channel SPI clock
		OUT	GPIO Output, Zone Detect 2. High: target exists; Low: No target
RX	31	IN	Single-ended receiver input port
GND	Thermal PAD, 2, 9, 11, 30, 32	GND	Ground

Note:

There are pin multiplexing functions in Pin 20, Pin 21, Pin 23, Pin 25, Pin26, Pin 27, Pin 28, and Pin 29.

5.3 Pin Mux function

The ICL1112 Pin 20, Pin 21, Pin 23, Pin 25 ~Pin 29 have multiple digital communication multiplexing functions.

Pin 23/Pin 24/Pin 25 should be properly set to Selected Chip Configuration mode during ICL1112 power up. Data output mode and CFAR function are configured by the ICL1112's registers configuration.

Table 5-2 Function mode selection setup - chip configuration setting

Pin 23	Pin 24	Chip Configuration Mode
Low	Low	UART
Low	High	I2C
High	Low	SPI
High	High	Reserved

When chip configuration mode is set as I2C communication, Pin 27 and Pin 28 should be set to configure the slave chip's address during ICL1112CL power up's chip settling time. Up to 4 devices can share the same I2C bus in I2C Configuration mode.

Table 5-3 I2C device address

Pin 27	Pin 28	I2C Slave Device Address
Low	Low	7'b010_0000
Low	High	7'b010_0001
High	Low	7'b010_0010
High	High	7'b010_0011

5.4 Standby Mode

The ICL1112 supports standby mode to achieve low power consumption. The ICL1112 enters the standby mode when Pin 25 is set to low or floating during power up period. After entering the standby mode, only power management unit, Osc. unit, and part of digital unit are activated.

The device exits the standby mode when registers configuration occurs.

Table 5-4 Working mode selection setup

Pin 25	Chip Configuration/Work Mode
Low	Standby Mode

5.5 Chip Configuration Pin States Configuration

The ICL1112 configuration states are fully determined by the external voltage applied on the Pin 23~Pin 25 during the chip settling time. Each pin configuration has 2 states: low and high. The pin can be set to "low" when connected to ground with a 3.3 kΩ resistor; and the pin can be set to "high" when connected to VDD with a 10 kΩ resistor. Pin 23 ~ Pin 25 can be floated when they are set to "high" as they are internally pulled up.

After the chip settling time, Pin 23~Pin 25's external applied configuration communication mode's selection control should be released, as the chosen pins' configuration communication mode or data communication mode is triggered.

6 Functional Description

6.1 Transceiver Section

The ICL1112 provides one transmitter, and the transmitter parameters can be set via I2C/SPI/UART configuration channel, and directly controlled by the waveform generator. The transmitter can deliver RF power of maximum 12 dBm via the TX port, and support programmable transmitter output power for system optimization.

The ICL1112 provides one receiver, which consists of LNA, mixer, LPF filters, PGAs, ADCs, and decimation filters. The baseband subsystem has one quadrature mixer, RX channels' IF and ADC chains to provide complex I and Q outputs for DSP processing.

6.2 Waveform Generator Section

The waveform generator provides a linear frequency chirp with frequency deviation from 0 MHz to 1000 MHz. CW mode is also supported in the waveform generator. The waveform generator provides a sequence of frequency chirps with precise timing. An indicative timing of each frequency chirp is shown in Figure 6-1.

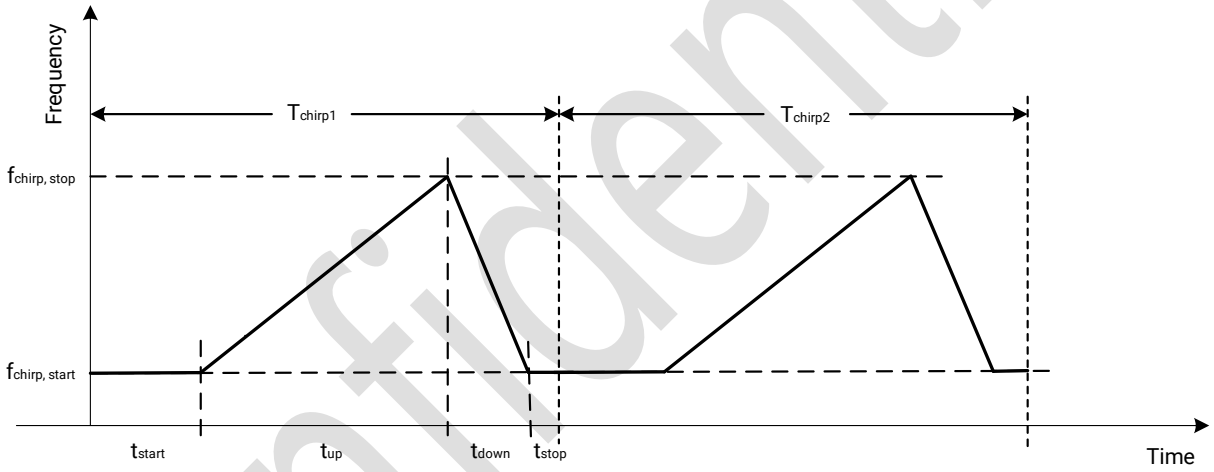


Figure 6-1 Timing parameters in a frequency chirp

The ICL1112 works in continuous sensing mode. Each frame starts from t_{pre}, during which the waveform generator is initialized to prepare the chirp generation. The t_{pre} is programable and typically 20 µs. Then the TX output port sends the given number of chirps for target sensing. After the last chirp of a frame, the ICL1112 can enter low power mode during the NOP time denoted as $t_{\_NOP}$ in Figure 6-2.

If the register 0x41 bit 4 is set to 0, the RF transceiver (PA, LNA) and baseband (ADC, LPF&PGA) circuits will automatically power down in each frame's NOP time $t_{\_NOP}$ and return to work at the next t_{pre} period. During the NOP time, PD time is ICL1112's fully power-down time. The ICL1112 takes $t_{\_2pd}$ time of typical 22 µs to turn to low power mode or vice versa.

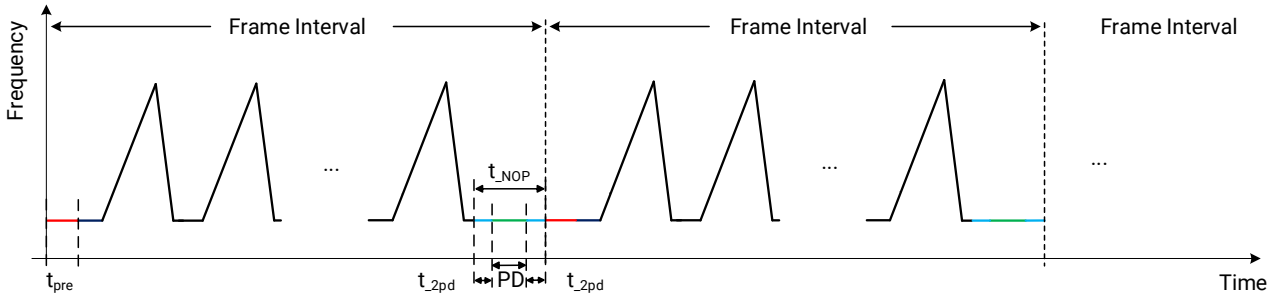


Figure 6-2 Continuous sensing mode

6.3 DSP Accelerator

The ICL1112 integrates Range FFT, Doppler FFT and DSP acceleration algorithm. A typical DSP flow diagram is shown in Figure 6-3.

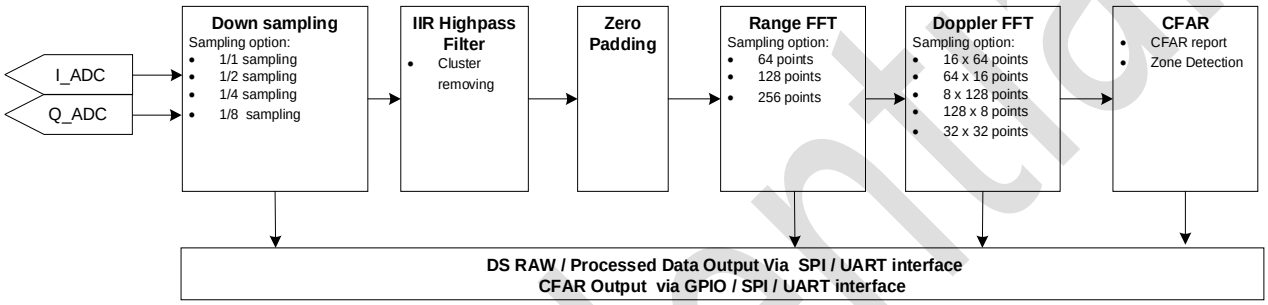


Figure 6-3 DSP accelerator data flow

The output of the hardware accelerator can be selected as DS RAW data, Range FFT data, Doppler FFT data, or CFAR data by the data output format configuration.

The I/Q data output from RX channel ADCs is processed by the DSP accelerator. In hardware accelerator, the raw data is down sampled firstly, and 4 down-sampling modes are supported by the decimation filter: 1/1, 1/2, 1/4, and 1/8 downing sampling. The down sampled data can be sent out as DS raw data, or go to the cluster removing filter (IIR High-pass Filter) and Zero padding. The whole data points number in one chirp is configurable.

To get better range accuracy, zero-padding process can be selected for data interpolation, the data sampling is illustrated as Figure 6-4. The ADC conversion can be configured to output certain data points, which start from T0 and end at T3. Keep Data Zone 2's data as original, and set Data Zone1 and Data Zone3's data to value of zero. Then the total data from Data Zone 1 to Data Zone 3 will be sent to Range FFT processing.

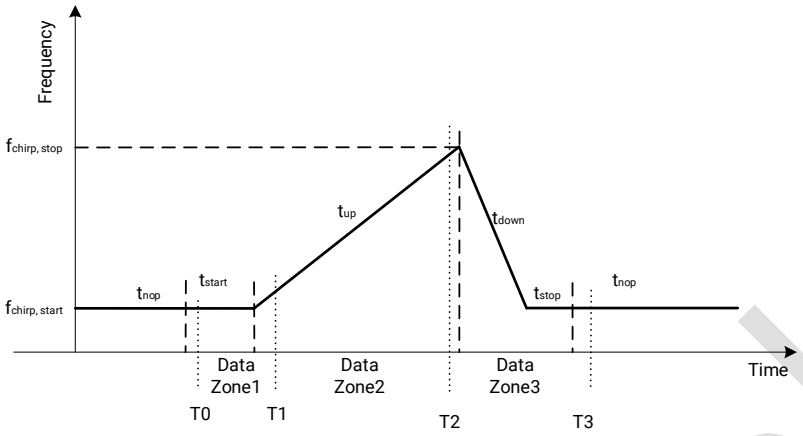


Figure 6-4 Zero padding data sampling diagram

Then the zero-padding data are sent to Range FFT processing block, with programmable FFT sizes of 64/128/256 points. If Doppler processing is selected, the output of Range FFT will be fed into the Doppler engine. The Doppler processing supports 16×64/64×16/8×128/128×8/32×32 sampling points. In both Doppler and Range FFT, Hanning, Hamming, Blackman or rectangular windows with corresponding width can be applicated before the transform. Finally, the CFAR engine can be selected as the last optional processing stage.

6.4 CFAR Function

The ICL1112 supports CFAR Report and Zone Detection.

If the CFAR Report function is enabled, CFAR detection is performed based on Doppler FFT data, as shown in Figure 6-3, and the CFAR report data will output via SPI/UART Interface.

If the Zone Detection function is enabled, there are maximum 4 subdivided detection zones at 4 output ports; the 4 subdivided detection output ports are located at Pin “SPI_DO” (Pin 27), Pin “TGT_DET” (Pin 28), Pin “SPI_SCLK” (Pin 29), and Pin “SPI_CSN” (Pin 26), from near to far. When a target is detected in a certain zone, the corresponding Pin will output a logical High, otherwise this pin keeps at logical Low.

6.5 Power Supply Section

The ICL1112 3.3 V power supply domain is based on an available supply voltage of nominal 3.3 V on the PCB board. The 3.3 V power supply is converted into a 1.6 V supply by means of on-chip DCDC circuits, or an external DCDC. The ICL1112 supports two power supply modes: single 3.3 V power supply mode, and dual power supply (3.3 V and 1.6 V) mode.

The 3.3 V power supply domain should be properly equipped with a 100 nF capacitor as close as possible to the power pins for better PSRR.

Pin DCDC_SW is an output pin of the internal DCDC buck converter, and it should connect to a 22 μH power inductor and a 22 μF capacitor as the internal DCDC’s output filter. The inductor and output capacitor together provide a low pass filter. The power inductor should be a low ESR power inductor, as in the reference of

SWPA252012S220MT. The output capacitor allows the use of ceramic capacitors with low ESR. These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

6.6 Temperature Sensor

A 10-bit temperature sensor is provided in ICL1112 for temperature monitoring.

6.7 Power detector

A 10-bit power detector sensor is provided for transmitter output power monitoring. The ICL1112 can achieve precise TX power control and power detection with this power detector. Application details can be found in *Application Guide for ICL1122/ICL1112 Power Detector and Temperature Sensor*.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Table 7-1 Absolute maximum ratings[1]

Parameter	Description	Min.[3]	Max.[3]	Unit
VDD_{max}	3.3 V power supply max input	-0.5	3.7	V
$V\_1.6_{max}$	1.6 V power supply (when internal DCDC is not used) max input	-0.5	3.7	V
RF_IN_{max}	Externally applied power on RX	-	0	dBm
RF_OUT_{max}[2]	Externally applied power on TX	-	16	dBm
Analog Input and Output voltage	Externally applied voltage at PLL_VC, REXT, XIN, XOUT, DCDC_SW ports	-0.5	3.7	V
Digital Input and Output voltage	Externally applied voltage at RSTN, I2C_SDA, I2C_SCL, C_SPI_MOSI, C_SPI_CSN, FUN_SEL, UART_TXD, SPI_CSN, SPI_DO, TGT_DET, SPI_SCLK ports	-0.5	3.7	V
T_J	Junction temperature range	-40	125	°C
T_{STG}	Storage temperature range	-40	125	°C

Note:

[1] All voltages with respect to ground.

[2] This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to Gamma = 1 can be applied on the TX output.

[3] Attention: Stresses exceeding those Max. and Min. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

7.2 ESD Ratings

Table 7-2 ESD ratings

Model		Value	Unit
V_{ESD}	HBM: Human body model	+/-2000[1]	V
	CDM: Charge device model	+/-500[2]	V

Note:

[1] According to ANSI/ESDA/JEDEC standard, Method JS-001-2017.

[2] According to ANSI/ESDA/JEDEC standard, Method JS-002-2014.

7.3 Thermal Resistance

Table 7-3 Thermal resistance

Parameter	Description	Min.	Typ.	Max.	Unit
$R_{\theta JA}$[1]	The junction-to-ambient thermal resistance	-	47	-	°C/W

Note:

[1] $T_j = T_A + R_{\theta JA} \times P_{total}$, where P_{total} is the power consumption of the chip and T_A is the environment temperature in the still air.

7.4 Recommended Operating Conditions

Table 7-4 Recommended operating conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD_A	3.3 V power supply for analog circuits	3.0	3.3	3.6	V
VDD	3.3 V power supply for DCDC and digital I/O circuits	3.0	3.3	3.6	V
V_T, V_R, V_A, V_D	1.6 V power supply when the internal DCDC is bypassed	1.5	1.6	1.7	V
VIH	Voltage input High	2.3	-	VDD	V
VIL	Voltage input Low	0	-	0.8	V
VOH	Voltage output High	2.45	-	VDD	V
VOL	Voltage output Low	0	-	0.45	V
T_J	Operating junction temperature range	-40	-	105	°C

7.5 Power Supply Characteristics

7.5.1 Power Supply Modes

The ICL1112 has internal low PSRR DCDC module and can support 2 power supply modes: 3.3 V single power supply mode, and 3.3 V/1.6 V dual power supply mode.

7.5.1.1 3.3 V Single Power Supply Mode

In 3.3 V single power supply mode, the ICL1112 can utilize the internal DCDC module of low PSRR, by connecting VDD_A and VDD to the external 3.3 V power supply, and connecting DCDC_SW to V_T/ V_R/V_A /V_D through an inductor.

7.5.1.2 3.3 V/1.6 V Dual Power Supply Mode

In 3.3 V/1.6 V dual power supply mode, the internal DCDC is bypassed by floating DCDC_SW. VDD_A and VDD are connected to the external 3.3 V power supply, and V_T/V_R/V_A/V_D are connected to the external 1.6 V power supply.

7.5.2 Power Consumption

Data in Table 7-5 are measured under 25°C ambient temperature, single power supply mode, applied external voltage refers to the typical value in Table 7-4.

Table 7-5 Average power consumption

Parameter	Description	Min.	Typ.	Max.	Unit
P_{total}	Average power consumption when internal DCDC is used, and all the circuits are in active mode.	-	300	420	mW
$P_{standby}$	Average power consumption when internal DCDC is used, and all the circuits work at standby mode.	-	28	38	mW
$P_{0.3\%dutycycle}$	Average power consumption with 0.3% duty cycle operation.		182		uW

Data in Table 7-6 are measured under 25°C ambient temperature when the internal DCDC is used, applied external voltage refers to typical value in Table 7-4.

Table 7-6 Maximum current ratings at power terminals

Parameter	Supply Name	Min.	Typ.	Max.	Unit
Current Consumption	VDD_A	-	-	23	mA
	VDD	-	-	110	mA

Data in Table 7-7 are measured under 25°C ambient temperature when the internal DCDC is bypassed.

Table 7-7 Maximum current ratings at power terminals

Parameter	Supply Name	Min.	Typ.	Max.	Unit
Current Consumption	VDD_A	-	-	22	mA
	VDD	-	-	12	mA
	V_T	-	-	112	mA
	V_R	-	-	33	mA
	V_A	-	-	30	mA
	V_D	-	-	10	mA

7.6 Dynamic Performance

Unless otherwise specified, the following conditions apply: single power supply mode, VDD and VDDA are connected to 3.3 V. T_{case} = 25 °C. Reference plane on PCB 1.6 mm from bump center; input and output load impedance at 50 Ω. All RF parameters are measured in an application board, relevant information is to be added.

Table 7-8 RF performance

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Z_Out	TX output load impedance	-	-	50	-	Ω
P_{max}_Out	TX maximum output power	-	-	11.9	-	dBm
F_Out	TX output frequency range	-	24	-	25	GHz
P_Out	TX output power range	-	0	-	12	dBm
S_{22}_RF_{out}	TX return loss	-	-	-8		dB
Z_In	RX input load impedance	-	-	50	-	Ω
P_{max}_RF_{in}	Max power feed into RX input	-	-	-	0	dBm
F_In	RX frequency range	-	24	-	25	GHz
S_{11}_RF_{in}	RX input return loss	-	-	-	-10	dB
NF	RX noise figure	SSB, including RF and ADC in RX@30 dB G_RF_{RX}	-	10.0	-	dB
IP1dB	RX RF Input 1 dB compression point (Rx chain including ADC)	30 dB gain, 24 GHz	-	-26	-	dBm
		24 dB gain, 24 GHz	-	-20	-	dBm
G_RF_{RX}	gain of RF in RX	-	15	-	31	dB

Table 7-9 Baseband performance

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Res_ADC	ADC resolution	-	-	16	-	bit
Fs	ADC conversion rate	-	-	2.5	-	MHz

Table 7-10 Pattern generator and PLL performance

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
F_Ref	PLL input reference frequency	-	-	25	-	MHz
BW_PLL	PLL bandwidth	-	60	120	240	kHz
PN_{1MHz}	Phase noise at 1 MHz offset @ TX output port	With the off-chip filter parameters as follow: R1=820 Ω, C3=4.7 nF C4=820 pF (BW_PLL=120 kHz)	-	-97	-91	dBc/Hz
BW_Chirp	FMCW chirp bandwidth	Measured @ TX output	-	0.25	1	GHz
R_Ramp	FMCW chirp ramp rate	BW_PLL=240 kHz, BW_Chirp=1 GHz	-	-	20	MHz/μs
Freq_err	rms frequency error during FMCW frequency modulation	BW_PLL=240 kHz, BW_Chirp=1 GHz R_Ramp=13 MHz/μs	-	1‰	-	-
		BW_PLL=240 kHz, BW_Chirp=250 MHz R_Ramp=3.3 MHz/μs	-	0.45‰	-	-

Table 7-11 DCDC performance

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{sw}	Internal DCDC switching frequency	Single power supply mode	400	500	650	kHz

7.7 Timing and Switching Characteristics

7.7.1 Start-up Sequence

The start-up sequence is depicted in Figure 7-1. If the ICL1112 works in single power supply mode, the power supply pins' power-up sequence requirements should be neglected, as V_T/V_R /V_A/V_D are supplied by internal DCDC and the power up sequences are controlled by the internal power management unit. If the ICL1112 works in dual power supply mode, the V_T, V_R, V_A and V_D pins should be powered up after VDD in roughly 1.2 ms. After a rough time of 3 ms (T_{start}), the crystal oscillator is stabilized. An interval of roughly 0.5 ms after T_{start}, the chip configuration and data communication interfaces are ready, the internal SYS_RSTn is released, the external pin mux function selection control can be released. Then, after the time of around 0.4 ms, the PLL synthesizer is enabled. Finally, after roughly 0.2 ms, all function blocks are ready.

The duration from VDD power up to the external Pin 23 ~ Pin 25 pin mux function selection control released and chip configuration and data communication ready is roughly 3.5 ms.

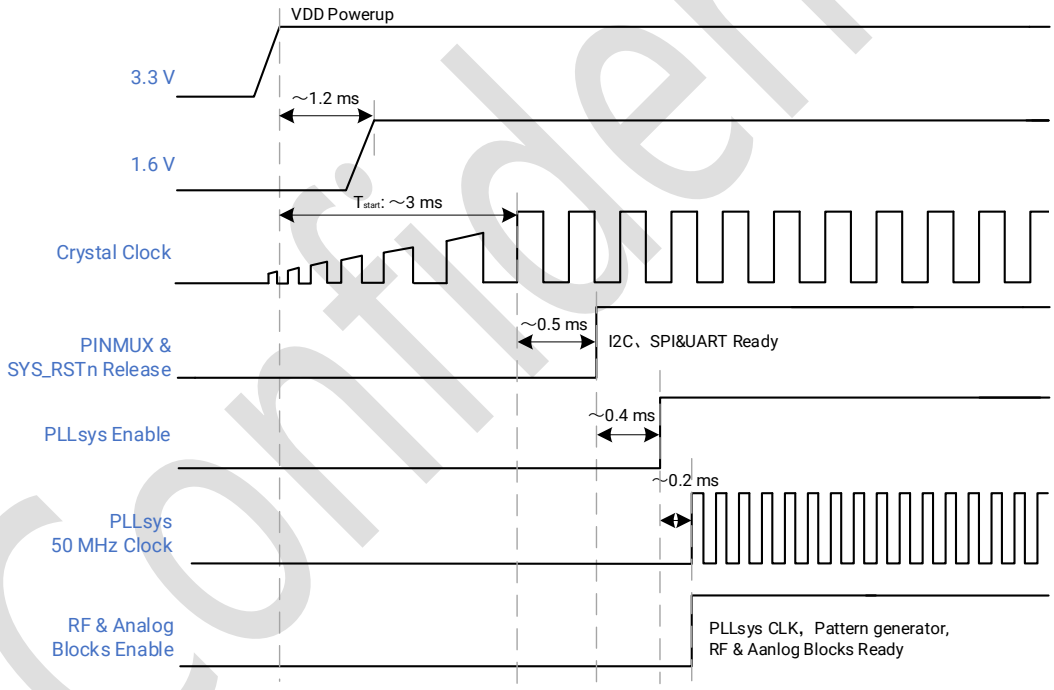


Figure 7-1 Power up timing and sequence

7.7.2 Hardware Reset Timing

Hardware reset requires an external reset pulse showed in Figure 7-2. If hardware reset is active, all the ICL1112 internal registers values will be reset to their default values, and all the chip's configurations need to be re-configured after the reset finishes.

Hardware reset will activate when Pin RSTN is triggered by logic low, and T_{RST} is recommended to be greater

than 2 ms.

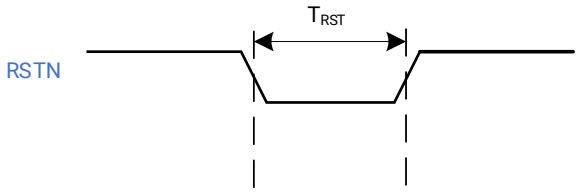


Figure 7-2 Reset pulse width

7.8 External Clock and Crystal Characteristics

The ICL1112 requires an external clock source (that is, a 25 MHz crystal or an external clock input) for initial boot and as a reference for the internal PLL hosted in the device. Since the feedback resistance is integrated on the chip, only a crystal and capacitors Ct1 and Ct2 need to be connected externally, in the case of fundamental mode oscillation. Figure 7-3 shows the crystal implementation.

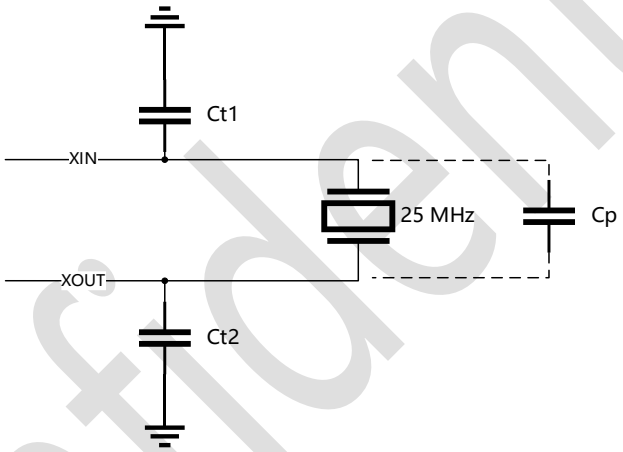


Figure 7-3 Crystal implementation

The load capacitors, Ct1 and Ct2 in Figure 7-3 should be chosen such that Equation 1 is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator XIN and XOUT pins.

$$C_L = \frac{Ct1 \times Ct2}{Ct1+Ct2} + Cp \qquad \text{Equation 1}$$

Table 7-12 shows the electrical characteristics of the clock crystal.

Table 7-12 Crystal electrical characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
f_P	Parallel resonance crystal frequency	-	25	-	MHz
C_L	Crystal load capacitance	5	10	20	pF
C_p	Crystal shunt capacitance	-	-	2	pF
ESR	Crystal ESR	-	-	50	Ω

Temperature range	Expected temperature range of operation	-40	-	85	°C
Frequency tolerance	Crystal frequency tolerance[1][2][3]	-50	-	50	ppm

Note:

[1] The crystal manufacturer's specification must satisfy this requirement.

[2] Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

[3] Crystal tolerance affects radar sensor accuracy.

The clock signal becomes available at the moment the crystal signal level stabilizes, typically 3 ms after the supply lines to the ICL1112 are activated.

An external AC coupled sine wave or DC coupled square wave clock signal may be applied to the ICL1112 as the reference clock. The clock is fed to XIN pin only, XOUT pin should be floated. The electrical characteristics of the external clock signal are shown in Table 7-13. The incoming clock signal should be AC-coupled to the XIN pin, using a 2-pF capacitor.

Table 7-13 External clock signal specifications

Parameter	Description	Min.	Typ.	Max.	Unit
fs	External clock signal frequency	-	25	-	MHz
Amp	AC clock signal amplitude	0.5	-	1.5	V(pp)
Duty cycle	Duty cycle of clock signal	-	50%	-	-
Frequency tolerance	Crystal frequency tolerance	-50	-	50	ppm
PN	Phase noise at 1 kHz	-	-	-135	dBc/Hz
	Phase noise at 100 kHz	-	-	-150	dBc/Hz
	Phase noise at 1 MHz	-	-	-150	dBc/Hz

8 Interface and Peripherals

The ICL1112 has 2 types of digital communication interfaces: chip configuration interface and data output interface.

8.1 Chip Configuration Communication Interface

The ICL1112 configuration communication interface is determined by Pin 23 and Pin 24 status during the power up period. The ICL1112 has 3 types of configuration communication modes: I2C, SPI, and UART.

8.1.1 I2C for Configuration

The I2C module works as a slave terminator, and has the following features:

- The I2C-interface is an I2C-bus compliant interface with open-drain pins;
- The I2C-bus interface supports Fast-mode with bit rate up to 400 kHz;
- Bidirectional data communication between masters and slaves;
- Support up to 4 I2C device addresses.

8.1.1.1 I2C Timing Characteristics

Table 8-1 I2C timing parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{scl}	SCL clock frequency	-	-	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	0.4	-	-	µs
t_{LOW}	Low time of the SCL clock	0.4	-	-	µs
t_{HIGH}	High time of the SCL clock	0.4	-	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	0.1	-	-	µs
$t_{HD;DAT}$	Data hold time	40	-	-	ns
$t_{SU;DAT}$	Data set-up time	50	-	-	ns
t_r	Rise time of both SDA and SCL signals	20	-	300	ns
t_f	Fall time of both SDA and SCL signals	20	-	300	ns
$t_{SU;STO}$	Set-up time for STOP conditions	0.1	-	-	µs
t_{BUF}	BUS free time between a STOP and START condition	1	-	-	µs

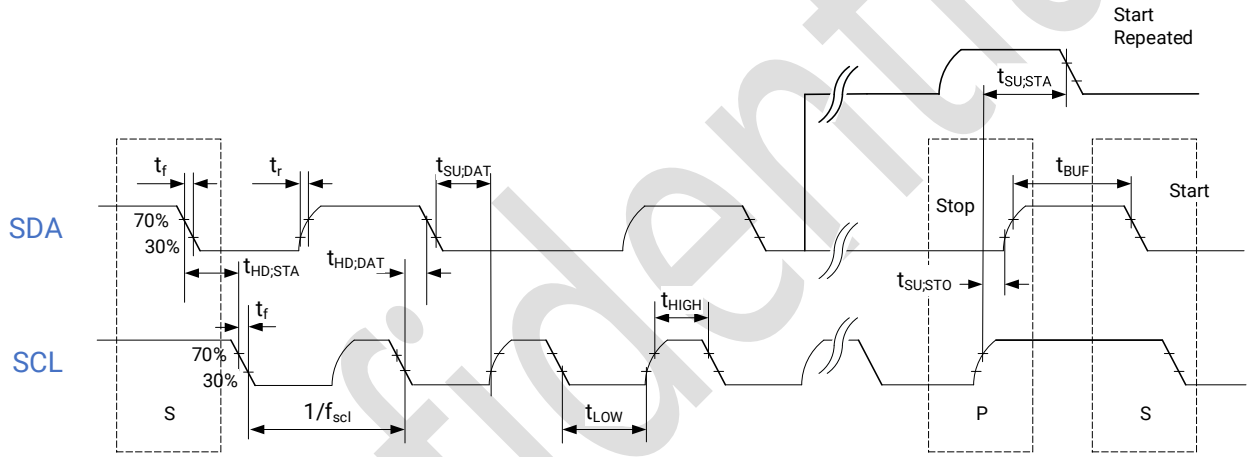


Figure 8-1 I2C timing diagram

The data on the SDA must be stable during the t_{HIGH}, and can only change when the clock signal is low.

Table 8-2 lists the acronyms used in I2C functionality.

Table 8-2 I2C abbreviations

Acronym	Description
SA[6:0]	The 7 bits slave address
SRA[7:0]	Slave Internal Register Address
DATA[x+7:x]	Data Word
R / $\overline{W}$	Read/Write (0 = data from master to slave, 1 = data from slave to master)
ACK	Acknowledgement
NACK	Non-Acknowledgement (=1)
S	Start condition (initiated by the master)
Sr	Repeated Start condition (initiated by the master)
P	Stop condition (initiated by the master)

8.1.1.2 I2C Interface Data Protocol

The ICL1112 Configuration_I2C interface operates in byte data format. The Start and Stop conditions are generated by the external master terminator, and depicted as S and P part in Figure 8-2. The first byte after the START condition consists of a 7-bit slave address followed by the R / $\overline{W}$ bit.

R / $\overline{W}$ = 0: The master writes data to the addressed slave.

R / $\overline{W}$ = 1: The master reads data from the slave.

One extra clock dedicated for acknowledgement (ACK) is inserted after each byte. If the ACK is inserted by the slave after the first byte from the master, it is followed by 8 bits of data from the transmitter (master or slave, depending on the R / $\overline{W}$ bit). After the data bits have been received, the receiver inserts an ACK bit.

To ignore the readback message, the master terminator must send a no-acknowledge (NACK) bit at the acknowledge clock time on the bus.

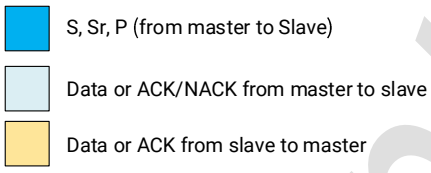


Figure 8-2 I2C color conventions

8.1.1.3 I2C Write

A typical I2C write for chip configuration is depicted in Figure 8-3.

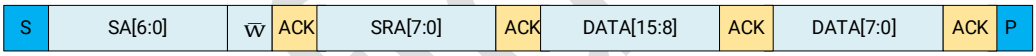


Figure 8-3 I2C configuration communication Write

8.1.1.4 I2C Read

In a read sequence (bit R / $\overline{W}$ = 1), after each data byte, the master responds with an acknowledgement (ACK). After the last data byte, the master responds with a non-acknowledgement (NACK). A typical I2C read for chip configuration is depicted in Figure 8-4.

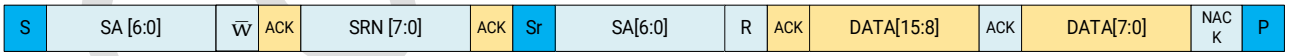


Figure 8-4 I2C configuration communication Read

8.1.2 SPI for Configuration

The ICL1112 chip configuration SPI supports full duplex communication and has the following features:

- Maximum SPI speed of 3.125 MHz;
- Synchronous serial communication;
- Slave mode operation at mode00.

8.1.2.1 Configuration SPI Interface Timing Characteristic

Table 8-3 Configuration SPI timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
$T_{c(sclk)}$	Clock period	320	-	-	ns
T_{sclk_high}	Clock high time	160	-	-	ns
T_{sclk_low}	Clock low time	160	-	-	ns
$T_{h(CSN)}$	Chip select hold time	320	-	-	ns
$T_{su(SI)}$	SPI MOSI input setup time	40	-	-	ns
$T_{h(SI)}$	SPI MOSI input data hold time	40	-	-	ns
$T_{a(SO)}$	SPI data output access time	0	-	-	ns
$T_{h(SO)}$	SPI data output hold time	40	-	-	ns
$T_{v(SO)}$	SPI MOSI data output valid time	-	-	120	ns
T_{cs_sclk}	SPI CSN setup time	160	-	-	ns
T_{sclk_cs}	SPI CSN hold time	160	-	-	ns
T_{cs_cs}	SPI CSN disable to next CSN enable time	320	-	-	ns
POL_{clk}	SPI clock polarity (CPOL)	-	0	-	-
ϕ_{clk}	SPI clock phase (CPHA)	-	0	-	-

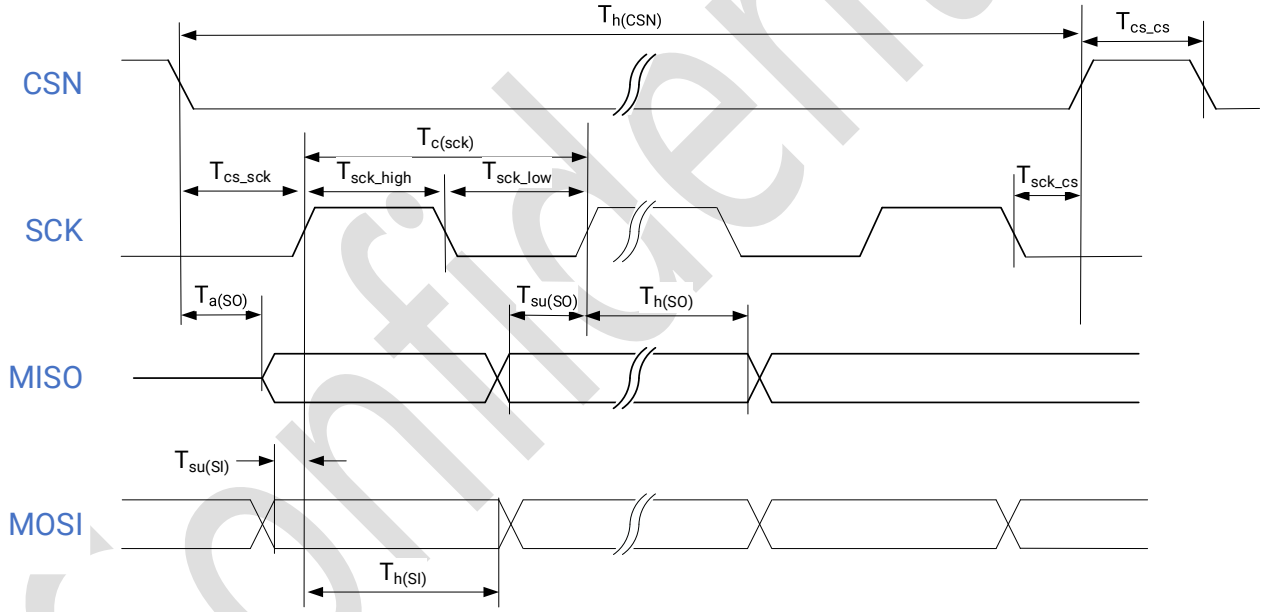


Figure 8-5 Configuration SPI interface timing diagram

8.1.2.2 Configuration SPI Interface Data Protocol

The ICL1112 configuration SPI interface works at 4-wire communication mode, the control is based on a combination of a single SPI protocol handler, with several register interfaces within each sub-block.

Pin nomenclature for interfacing to a host MCU is as follows: “SCLK” is the serial clock input at a maximum bus signaling rate of 3.125 MHz; “MOSI” (Master Out Slave In) is the serial input to write serial data into ICL1112; “MISO” (Master In Slave Out) is the serial output for data to be read from ICL1112; and “CSN” (Chip Select) is the select pin for write and read operations.

The ICL1112 SPI operates in byte data format. The data frame starts from R / $\overline{W}$, then 7 bits A0~A6 follows, 2 bytes data will be read or written in communication process.

R / $\overline{W}$ = 0: The master writes data to the addressed slave.

R / $\overline{W}$ = 1: The master reads data from the slave.

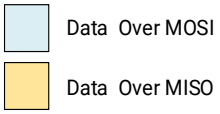


Figure 8-6 SPI color conventions

8.1.2.3 SPI Write

The SPI interface can be used to write into a single 16-bit register. A typical SPI write for a chip configuration data is depicted in Figure 8-7. The write operation starts with R / $\overline{W}$ bit, followed by the Register address (7 bits), and a payload message of 16-bit.

Figure 8-7 SPI configuration Write

8.1.2.4 SPI Read

The MISO interface timing is shown in Figure 8-8. The interface protocol shown below is valid only if the first bit of MOSI (R / $\overline{W}$ bit) is set to '1'.

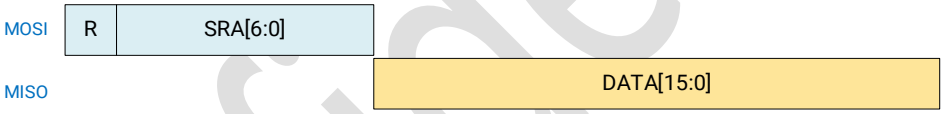


Figure 8-8 SPI configuration Read

8.1.3 UART for Configuration

The ICL1112 chip configuration UART interface has both TX and RX lane, and the typical data communication speed is 115200 bps.

8.1.3.1 Configuration UART Interface Timing Characteristic

Table 8-4 Configuration UART interface timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
Bd	Baud Rate	-	115200	-	bps

8.1.3.2 Configuration UART Interface Data Protocol

The ICL1112 configuration SPI interface is based on a combination of a single UART protocol handler and several register interfaces within each sub-block.

Pin nomenclature for interfacing to a host controller is as follows: "Configuration_UART_RX" is the serial input to write serial data into ICL1112; "Configuration_UART_TX" is the serial output for data to be read from ICL1112.

The ICL1112 UART interface operates in asynchronous communication mode with no clock pin. The data frame starts from a start bit ('0'), then followed with 8 bits data payload with additional one parity bit, and ends

with one stop bit.

During UART configuration operation, data sent to ICL1112 should contain one parity bit and the ICL1112 does not check the parity; data sent from ICL1112 will add 1-bit odd parity.

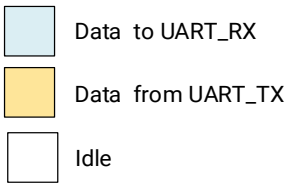


Figure 8-9 UART color conventions

8.1.3.3 Configuration UART Write

The UART interface can be used to write into a single 16-bit register. A typical UART chip configuration is depicted in Figure 8-10. The configuration operation command is composed of 3 sections: the first section sends the 7-bit slave address and 1-bit R / $\overline{W}$; the next two sections write the data values to the slave address. A payload message of 16-bit data is divided into two sections (low bits and high bits), and follows the rule that starts from a start bit ('0'), with 8 bits data follow, and ends with a parity check bit and a stop bit.

The data Write or Read enable bit located at slave address section.

R / $\overline{W}$ = 0: The master writes data to the addressed slave.

R / $\overline{W}$ = 1: The master reads data from the slave.

S: start bit.

SRA: slave internal register address.

PA: parity check bit.

P: stop bit.

I: idle bits.

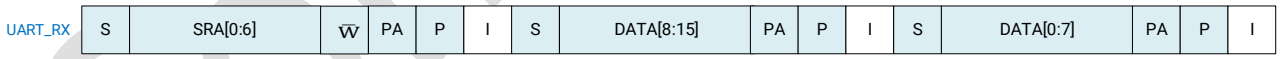


Figure 8-10 UART configuration Write

8.1.3.4 Configuration UART Read

The Read operation timing is shown in Figure 8-11. The interface protocol shown below is valid only if the first bit of UART_RX (R / $\overline{W}$ bit) is set to 'R'.

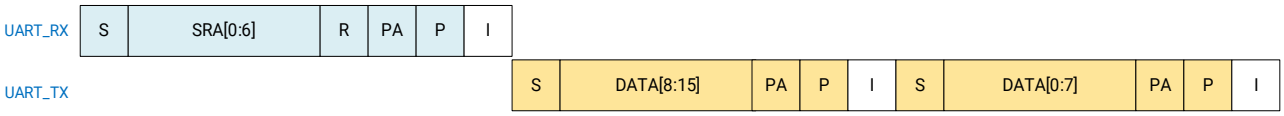


Figure 8-11 UART configuration Read

8.2 Chip Data Communication Interface

The ICL1112 data communication is determined by the register setting. The ICL1112 has 2 types of data communication modes: SPI, and UART. SPI and UART interfaces send the DS RAW/DSP processed data out to the receiver.

8.2.1 SPI for Data Communication

The ICL1112 chip data communication SPI interface can work in both master mode and slave mode. By default, Pin 27 “SPI_DO” (MOSI) transmits RX’s data. The master mode or slave mode is configurable by the register setting.

The SPI interface supports data output with DS RAW / frames of FFT data flowing from the master to the slave, and has the following features:

- Maximum SPI speed of 25 MHz in master mode;
- Maximum SPI speed of 7 MHz in slave mode;
- Mode00 operation.

8.2.1.1 SPI Interface Timing Characteristic

Table 8-5 Data Communication SPI timing characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$T_{c(sclk)}$	clock period	Master mode	40	-	2560	ns
		Slave mode	140	-	-	ns
T_{sclk_high}	clock high time	Master mode	13	-	-	ns
		Slave mode	70	-	-	ns
T_{sclk_low}	clock low time	Master mode	27	-	-	ns
		Slave mode	70	-	-	ns
$T_{\_h(MO)}$	SPI data output hold time	Master mode	0	-	-	ns
$T_{\_h(SO)}$		Slave mode	40	-	-	ns
$T_{\_v(MO)}$	SPI DO data output valid time	Master mode	15	-	-	ns
$T_{\_v(SO)}$		Slave mode	-	-	70	ns
$T_{\_a(SO)}$	Data output access time	Slave mode	0	-	-	ns
T_{cs_scl}	SPI CSN setup time	Master mode	60	-	-	ns
		Slave mode	70	-	-	ns
T_{scl_cs}	SPI CSN hold time	Master mode	40	-	-	ns
		Slave mode	70	-	-	ns
T_{cs_cs}	SPI CSN disable to next CSN enable time	Master mode	120	-	-	ns
		Slave mode	210	-	-	ns
T_{rdy}	data is ready for transmission	Slave mode	0	-	-	-

POL_{clk}	SPI clock polarity (CPOL)	Master mode Slave mode	-	0	-
ϕ_{clk}	SPI clock phase (CPHA)	Master mode Slave mode	-	0	-

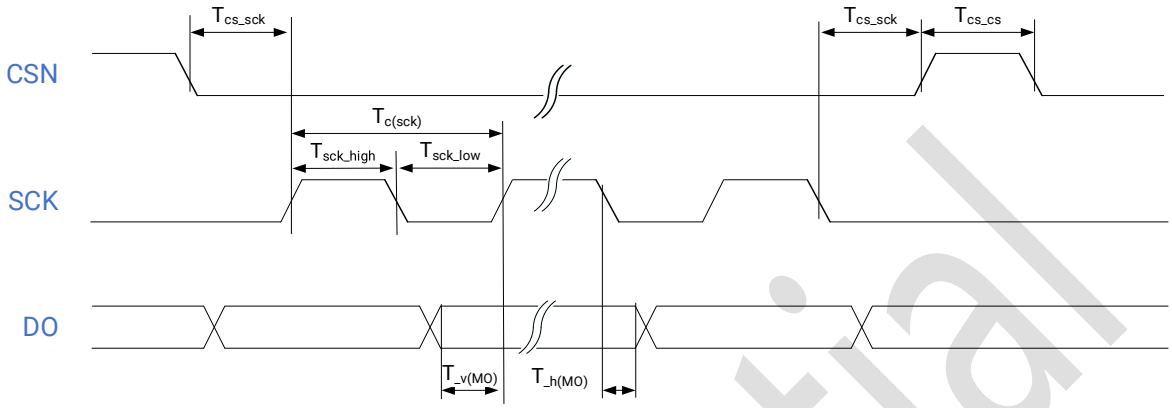


Figure 8-12 Data communication SPI timing diagram – master mode

In slave mode, Pin 25 will send logic “1” out as data output ready indication. When DO data are ready for transmit at Pin 27, the external master will send CSN and SCK signal to the ICL1112’s Pin 26 and Pin 29. Then the data can output following the SPI slave mode timing shown in Figure 8-13. After the last bit of the data, the external SCK signal changes to logic “0”, the external CSN changes to logic “1” according to the data length.

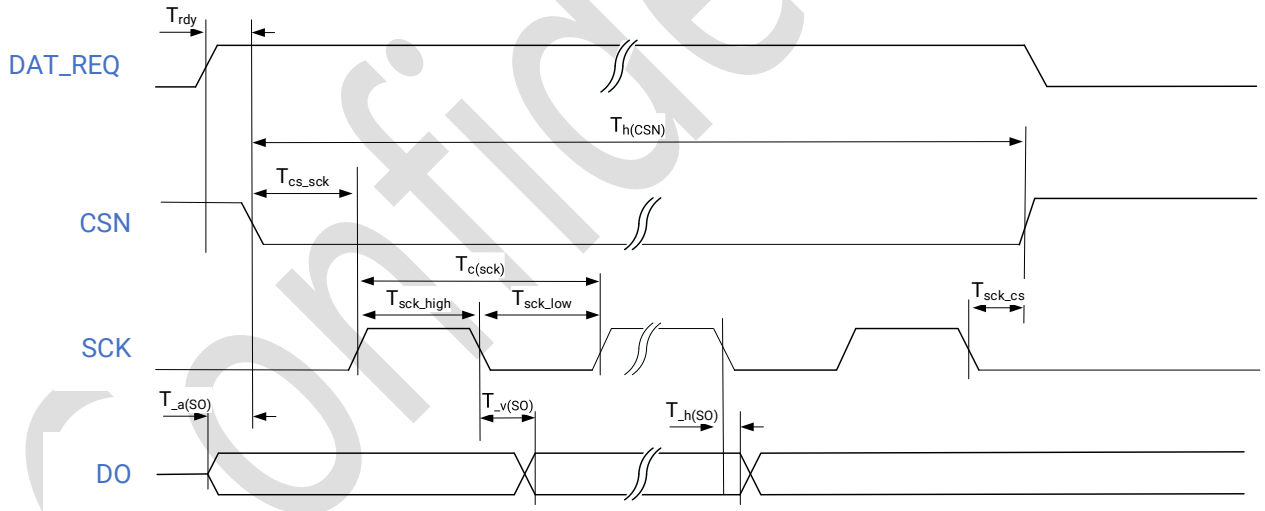


Figure 8-13 Data communication SPI timing diagram - slave mode

The data that SPI outputs are not guaranteed during the period of chip configuration. All the data that transmitted out through the DATA_SPI channel follow the format shown in Figure 8-14.

Figure 8-14 DATA channel transmission

8.2.1.2 SPI Output for Range FFT

When Range FFT data SPI output mode is selected by chip configuration command, the chip will transmit Range FFT data. Pin nomenclature for interfacing is as follows: Pin 29 “SPI_SCLK” is the serial clock output; Pin 27 “SPI_DO” is RX port’s serial data from ICL1112; and Pin 26 “SPI_CSN” (Chip Select) is the select pin for read operations.

The ICL1112 data communication SPI operates in 32-bit format. The data frame starts with the header Dword (32 bits); then all the FFT data is sent out, with the high 16 bits represent real part of the FFT data, and the low 16 bits represent imaginary part of the FFT data; finally, the tail Dword (32 bits) will valid the check_sum and terminate the data output.

The data output is MSB first and the Range FFT data type is signed integer. Table 8-6 illustrates the Range FFT data format over DO.

Table 8-6 Range FFT data frame format over DO

Header[Dword 0]	'b1010 1010	'b 0	'b 011	FFT_chirp_index1 (bit 7:0, 8)[19:11][1]	CFG_FFT_TX_MAX[10:0][2]		
Data[Dword 1]	FFT real data 0[31:16]				FFT Imaginary data 0[15:0]		
Data[Dword 2]	FFT real data 1[31:16]				FFT Imaginary data 1[15:0]		
Data[Dword ⋯]	FFT real data ⋯[31:16]				FFT Imaginary data ⋯[15:0]		
Data[Dword m]	FFT real data m-1[31:16]				FFT Imaginary data m-1[15:0]		
Tail[Dword m+1]	Check_sum[31:16][3]				FFT_FRAME_INDEX [15:12][4]	'b 00 [5]	CFG_MSG [9:8][6]	'b 0101 0101

Note:

[1] FFT_chirp_index1(bit 7:0, 8)[19:11]: The chirp sequence number in one frame, start from “0” in each frame. MSB is located at bit 11, then bit 19:12 is from MSB-1 to LSB.

[2] CFG_FFT_TX_MAX[10:0]: The number of m (the total FFT output points) +1 in this chirp.

[3] Check_sum[31:16]: The sum of all data in this chirp, and equals to the value of low 16 bits sum result.

[4] FFT_FRAME_INDEX[15:12]:The frame num counter, start from 0.

[5] Default 0, can act as frame_cnt[1:0] with extra configuration.

[6] CFG_MSG[9:8]: User defined bits.

8.2.1.3 SPI Output for Doppler FFT

When Doppler FFT data SPI output mode is selected by chip configuration command, the chip will output Doppler FFT data. Pin nomenclature for interfacing is as follows: Pin 29 “SPI_SCLK” is the serial clock output; Pin 27 “SPI_DO” is RX port’s serial data from ICL1112; and Pin 26 “SPI_CSN” (Chip Select) is the select pin for read operations.

The ICL1112 data communication SPI operates in 32-bits format. The data frame starts from the header Dword

(32 bits); then all the Doppler FFT data are sent out, with the high 16 bits represent real part of the Doppler FFT data, and the low 16 bits represent imaginary part; finally, the tail Dword (32 bits) will valid the check_sum and terminate the data output.

The data output is MSB first and the Doppler FFT data type is signed integer. Table 8-7 illustrates the Doppler FFT data format over DO.

Table 8-7 Doppler FFT data frame format over DO

Header[Dword 0]	'b1010 1010	'b 0	'b 100	DFFT_chirp_index1(bit 7:0, 8)[19:11][1]	DW_LEN[10:0][2]
Data[Dword 1]	DFFT real data 0[31:16]			DFFT imaginary data 0[15:0]	
Data[Dword 2]	DFFT real data 1[31:16]			DFFT imaginary data 1[15:0]	
Data[Dword ⋯]	DFFT real data ⋯[31:16]			DFFT Imaginary data ⋯[15:0]	
Data[Dword m]	DFFT real data m-1[31:16]			DFFT Imaginary data m-1[15:0]	
Tail[Dword m+1]	Check_sum[31:16][3]			FFT_FRAME_INDEX[15:12][4]	'b 00 CFG_MSG[9:8][5] 'b 0101 0101

Note:

[1] DFFT_chirp_index1(bit 7:0, 8)[19:11]: The chirp sequence number in one frame, start from "0" in each frame. MSB is located at Frame data's bit 11, then bit 19:12 is from MSB-1 to LSB.

[2] DW_LEN[10:0]: Doppler FFT data num counter, start from 0.

[3] Check_sum[31:16]: The sum of Doppler FFT data in this frame, and equals to the value of low 16 bits sum result.

[4] FFT_FRAME_INDEX[15:12]: The frame num counter, start from 0.

[5] CFG_MSG[9:8]: User defined bits.

8.2.1.4 SPI Output for DS RAW

When DS RAW data SPI output mode is selected by chip configuration command, the chip will output DS RAW data. Pin nomenclature for interfacing is as follows: Pin 29 "SPI_SCLK" is the serial clock output; Pin 27 "SPI_DO" is RX's serial data from ICL1112; and Pin 26 "SPI_CSN" (Chip Select) is the select pin for read operations.

The ICL1112 can output down-sampled RAW data (down sampling rate: 1/2, 1/4, 1/8). DS RAW data communication SPI operates in 32-bit format. The data frame starts with the header Dwords; then all the DS RAW data are sent out, with the high 16 bits represent real part of the DS RAW data, and the low 16 bits represent imaginary part; finally, the tail Dwords will valid the check_sum and terminate the data output.

The data output is MSB first and the DS RAW data type is signed integer. Table 8-8 illustrates the DS RAW data format over DO.

Table 8-8 DS RAW data frame format over DO

Header[Dword 0]	'b1010 1010	'b 0	'b 010	RAW_chirp_cnt (bit 7:0, 8) [19:11][1]		RAW_DATA_cnt[10:0][2]
Data[Dword 1]	DS RAW real data 0[31:16]			DS RAW Imaginary data 0[15:0]		
Data[Dword 2]	DS RAW real data 1[31:16]			DS RAW Imaginary data 1[15:0]		
Data[Dword ...]	DS RAW real data ...[31:16]			DS RAW Imaginary data ...[15:0]		
Data[Dword m]	DS RAW real data m-1[31:16]			DS RAW Imaginary data m-1[15:0]		
Tail[Dword m+1]	Check_sum[31:16][5]			RAW_FRAME_INDEX [15:12][6]	'b 00	CFG_ MSG [9:8][7]	'b 0101 0101

Note:

[1] RAW_chirp_cnt (bit 7:0, 8)[19:11]: The chirp sequence number in one frame, start from "0" in each frame. MSB is located at Frame data's bit 11, then bit 19:12 is from MSB-1 to LSB.

[2] RAW_DATA_cnt[10:0]: The number of m (the total items of DS RAW data) in this chirp.

[3] Check_sum[31:16]: The sum of all data in this frame, and equals to the value of low 16 bits sum result.

[4] RAW_chirp_cnt[11:8]: The chirp sequence number in one frame, it equals to RAW_chirp_cnt[19:11]'s low 4 bits value.

8.2.1.5 SPI Output for CFAR Report

The ICL1112 can transmit CFAR Report with data SPI, where Pin 27 is the data output bus. The output is MSB first and the CFAR Report type is signed integer.

Table 8-9 CFAR Report frame format

Header[Dword 0]	'b1010 1010	'b1	'b 000	'b 0 0000 0000		CFG_LEN_RPT[10:0][1]	
Data[Dword 1]	'b 0 0000 0000		CFAR_PMAX3_didx[22:16] [2]		'b 0 0000 0000		CFAR_PMAX3_ridx[6:0][3]
Data[Dword 2]	CFAR_PMAX3_value[31:0][4]						
Data[Dword 3]	'b 0 0000 0000		CFAR_PMAX2_didx[22:16]		'b 0 0000 0000		CFAR_PMAX2_ridx[6:0]
Data[Dword 4]	CFAR_PMAX2_value[31:0]						
Data[Dword 5]	'b 0 0000 0000		CFAR_PMAX1_didx[22:16]		'b 0 0000 0000		CFAR_PMAX1_ridx[6:0]
Data[Dword 6]	CFAR_PMAX1_value[31:0]						
Data[Dword 7]	'b 0 0000 0000		CFAR_PMAX0_didx[22:16]		'b 0 0000 0000		CFAR_PMAX0_ridx[6:0]
Data[Dword 8]	CFAR_PMAX0_value[31:0]						
TAIL[Dword 9]	Check_sum[31:16][5]				DPL_frame_cnt [15:12][6]	'b 00	CFG_ MSG [9:8][7]	'b 0101 0101

Note:

[1] CFG_LEN_RPT[10:0]: The length of Data payload; max value is 27.

[2] CFAR_PMAXm_didx[22:16]: Doppler FFT CFAR location, Doppler FFT index; PMAXm is from PMAX3 to PMAX0, and related to the 4 subdivided detect zones.

[3] CFAR_PMAXm_ridx[6:0]: Doppler FFT CFAR location, Range FFT index; PMAXm is from PMAX3 to PMAX0, and related to the 4 subdivided detect zones.

[4] CFAR_PMAXm_value[31:0]: Doppler FFT CFAR value; PMAXm is from PMAX3 to PMAX0, and related to the 4 subdivided detect zones.

[5] Check_sum[31:16]: The sum of all data in this frame, and equals to the value of low 16 bits sum result.

[6] DPL_frame_cnt[15:12]: Doppler frame num counter, starts from 0.

[7] CFG_MSG[9:8]: User defined bits.

8.2.2 UART Output for Data Communication

The ICL1112 data communication UART interface only has TX lane, and the electrical characteristics are listed in Table 8-10.

Table 8-10 Data communication UART interface electrical characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Bd	Baud Rate	4800	-	256000	bps

The ICL1112 DATA_UART_TX interface can also output Data SPI mode DATA_SPI_DO's data, including Range FFT data, Doppler FFT data and CFAR report. The DATA_UART_TX sends out the data with odd parity bit. The format is from DW0's highest byte to the lowest byte, then goes to the next DW, until reaches the last DW(DWx). Each byte is from LSB to MSB.

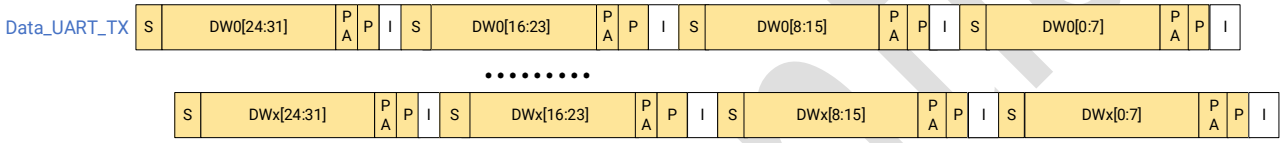


Figure 8-15 UART output data timing

9 Application Information

9.1 Application Schematic

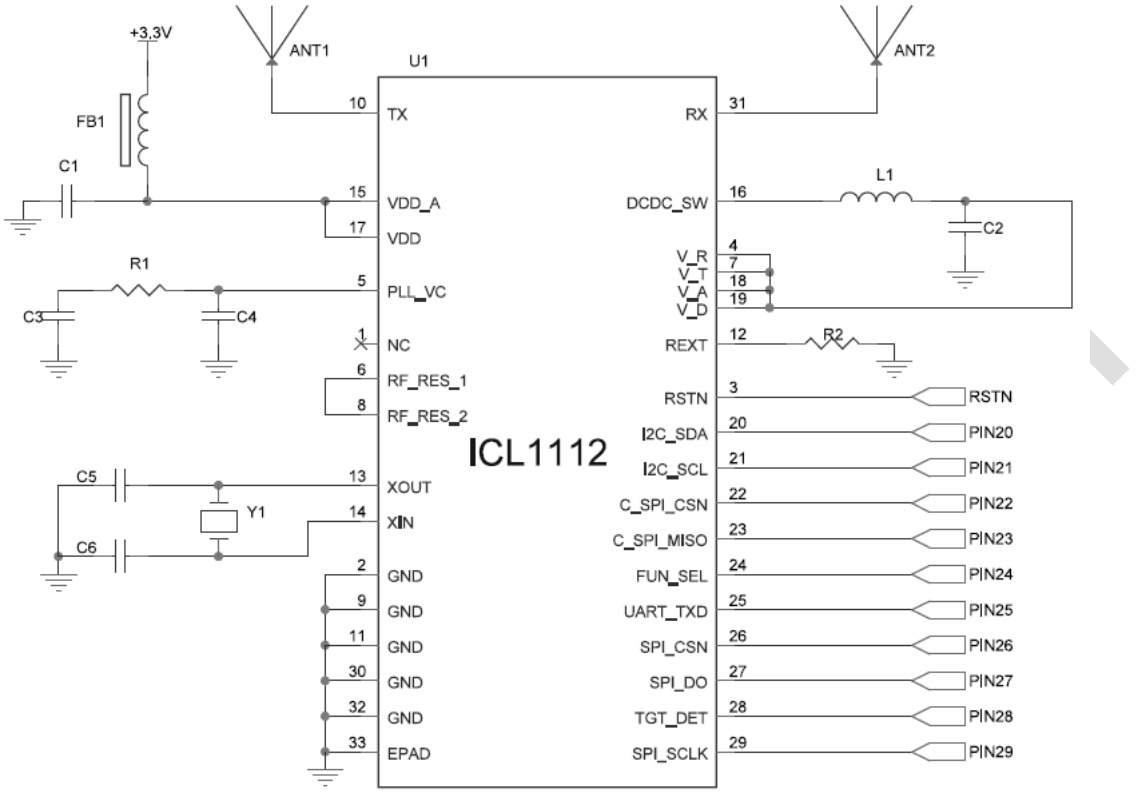
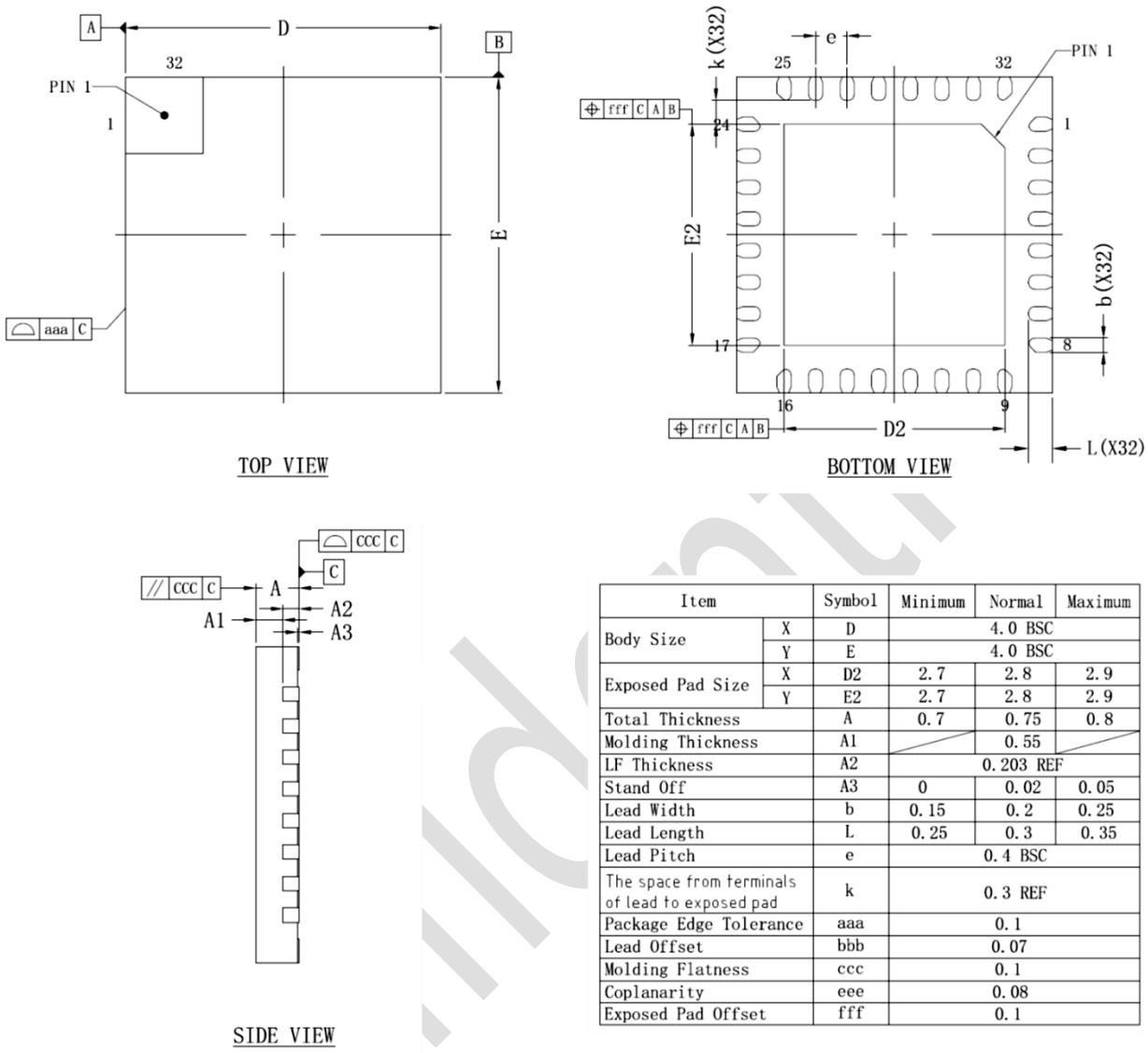


Figure 9-1 mmWave sensor application schematic

Table 9-1 External component suggestions

Component	Description	Value	Remarks
ANT1, ANT2	PCB patch antenna	24 GHz antenna	-
FB1	ferrite bead	GZ1005D310TF	-
C1	ceramic capacitor	100 nF	X7R
C2	DCDC output ceramic capacitor	22 μF	X5R
L1	DCDC output power inductor	22 μH	SWPA252012S220MT, ±20%, DCR < 1.7 Ω, Isat > 500 mA
R1	loop filter resistor	820 Ω	±5%
C3	loop filter ceramic capacitor	4.7 nF	±5%, X7R
C4	loop filter ceramic capacitor	820 pF	±5%, X7R
R2	resistor	12.4 kΩ	±1%
C5, C6	capacitor	12 pF	±5%, C0G
Y1	crystal	25 MHz	<50 ppm

10 Package Outline



Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		4.0 BSC	
	Y	E		4.0 BSC	
Exposed Pad Size	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
Total Thickness		A	0.7	0.75	0.8
Molding Thickness		A1		0.55	
LF Thickness		A2		0.203 REF	
Stand Off		A3	0	0.02	0.05
Lead Width		b	0.15	0.2	0.25
Lead Length		L	0.25	0.3	0.35
Lead Pitch		e		0.4 BSC	
The space from terminals of lead to exposed pad		k		0.3 REF	
Package Edge Tolerance		aaa		0.1	
Lead Offset		bbb		0.07	
Molding Flatness		ccc		0.1	
Coplanarity		eee		0.08	
Exposed Pad Offset		fff		0.1	

Figure 10-1 Package description

11 Handling Information

ESD CAUTION

ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

12 Revision History

Revision	Date	Data Sheet Status	Contents
0.1	2023/1/15	Objective Data Sheet	Initial draft.
0.2	2023/7/5	Objective Data Sheet	Functionality description added, Measurement data updated.
0.3	2023/7/13	Objective Data Sheet	Zero padding illustrated; Data SPI slave mode added, and correlated pin name changed; PLL, R_RAMP, linearity updated; Add the maximum PN value; NF typical value modified; Add zero padding description and illustration.
0.4	2023/8/9	Objective Data Sheet	Add chirp linearity in Main Features; Add smart lock/ring bell in Applications; Add 0.3% duty cycle power dissipation.
1.0	2023/8/24	Product Data Sheet	Modified descriptions in Applications block; Modified data format in Table 8-8; Modified description of Freq_err in Table 7-10.
1.1	2023/9/9	Product Data Sheet	Add TX return loss in Table 7-8; Add description on power detector in Main Features; Modified value for low power mode in Main Features, power consumption in Table 7-5, and data hold time in Table 8-1. Modified description on low power in Main Features;

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