

Data Sheet Sep 21 2018 Rev 3.1



Introduction

The 802.11b/g/n + BT 4.1 Wireless Sip module WM-BN-BM-26_A which refers as "SiP 3 in one module" is a small size module based on QFN package that provides full function of 802.11b/g/n with Bluetooth 4.1 in a tiny module via 59 pins LGA Footprint.

This multi-functionality and board to board physical interface provides SDIO v3.0/GSPI interfaces for Wi-Fi, UART/PCM for Bluetooth.

The small size & low profile physical design make it easier for system design to enable high performance wireless connectivity without space constrain. The low power consumption and excellent radio performance make it the best solution for OEM customers who require embedded 802.11b/g/n single-band Wi-Fi + Bluetooth features, such as, Wireless PDA, Smart phone, MP3, PMP, slim type Notebook, VoIP phone etc.

The module is based on Cypress 43438 chipset. The Radio architecture & high integration MAC/BB chip provide excellent sensitivity. The module is designed as a single dual-band antenna shared between Wi-Fi and Bluetooth for the application of small size hand held device.

In addition to WPA, WPA2 and TKIP, AES, CCX, WPS is supported to provide the latest security requirement on your network.

For the software and driver development, USI provides extensive technical document and reference software code for the system integration under the agreement of Cypress International Ltd.

Hardware evaluation kit and development utilities will be released base on listed OS and processors to OEM customers.

Features

- Support explicit IEEE 802.11n transmit beamforming.
- Supports 20 MHz bandwidth channels with optional SGI (256QAM modulation).
- Full IEEE 802.11b/g/n legacy compatibility with enhanced performance.
 - Lead Free design which supporting Green design requirement, RoHS Compliance, and halogen-free.
 - Support a single-band antenna shared between Wi-Fi and Bluetooth.
- Small size suitable for low volume system integration.Low power consumption & excellent power management performance extend battery life.
- 2.412-2.484 GHz SKU for worldwide market.
- Easy for integration into mobile and handheld device with flexible system configuration and antenna design.



	Change Sheet					
Boy	Date			Description of change	Prepared by	
nev.	Date	Page	Par	Change(s)		
1.0	2014.11.06	All	All	Preliminary version for Review	Aaron Hung & Ven Chen	
1.1	2014.11.12			Update the thickness of pcb board	Aaron Hung & Ven Chen	
1.2	2014.11.13			Update the supply of Vbat	Aaron Hung & Ven Chen	
1.3	2014.11.14			Update the min. spec of supply Vbat to 3.2V	Aaron Hung & Ven Chen	
1.4	2015.01.05			Update the HW Specifications	Aaron Hung & Ven Chen	
1.5	2015.04.07			Update the HW Specifications	Aaron Hung & Ven Chen	
1.6	2015.05.13			Update 4.9.1(pag27) Update4.10.1(pag28)	Aaron Hung & Ven Chen	
1.7	2015.05.29			Add P/N (pag1)	Aaron Hung & Ven Chen	
1.8	2015.06.30			Update 4.1.2(pag 9) Update 4.2.3(pag 10) Update 4.10 (pag 29)	Aaron Hung & Ven Chen	
1.9	2015.09.16			Add Ordering Information in Front Page	Aaron Hung & Ven Chen	
1.91	2016.02.23			Add B/G/N and BT TX Max, spec Add B/G/N and BT RX Min, spec.	Aaron Hung & Ven Chen	
2.0	2015.10.30	9		Update operating temp to -30 degrees 70 degrees	Jason	
2.1	2016.02.23			Update 4.2.3 (pag 9,10)	Aaron Hung & Ven Chen	
3.1	2018.09.21	9,37		1.Add a range of operating temperature. 2.Update recommended reflow profile.	Ven Chen	

TABLE OF CONTENTS

1	INTRODUCTION	2
2	FEATURES	2
1	BLOCK DIAGRAM	
2	DELIVERABLES	
3	REFERENCE DOCUMENTS	8
4	TECHNICAL SPECIFICATION	9
	4.1 ABSOLUTE MAXIMUM RATING	9
	4.2 RECOMMENDABLE OPERATION CONDITION	9
	4.2.1 TEMPERATURE, HUMIDITY	9
	4.2.2 VOLTAGE	9
	4.2.3 CURRENT CONSUMPTION	9
	4.3 WIRELESS SPECIFICATIONS	11
	4.4 RADIO SPECIFICATIONS 802.11B/G/N	11
	4.4.1 802.11B TRANSMIT	11
	4.4.2 802.11G I RANSMIT	12
	4.4.3 802.11N IRANSMII – H120	
	4.4.4 802.11B RECEIVER	
	4.4.5 802.11G RECEIVER	13 12
		13 14
		14 1/
	4.7 BEEERENCE CIRCUIT	14 15
	4.8 TIMING DIAGRAM OF INTERFACE	15 16
	4.8.1 CONTROL SIGNAL TIMING DIAGRAMS	10 16
	4.8.2 UART TIMING	
	4.8.3 SDIO TIMING	
	4.8.4 PCM TIMING	21
	4.9 FREQUENCY REFERENCES	
	4.9.1 EXTERNAL 32.768kHz LOW-POWER OSCILLATOR	
	4.10 DIMENSIONS, WEIGHT AND MOUNTING	
	4.10.1 DIMENSION & MODEL CODE	
5	LEGAL, REGULATORY & OTHER TECHNICAL CONSTRAINTS.	29
6	PIN OUT AND PIN DESCRIPTION	30
U		

UIDELINE TO PERFORM SMT WITH MODULE	
PCB FOOTPRINT RECOMMENDATION	
RECOMMENDED REFLOW PROFILE	
ACKAGE AND STORAGE CONDITION (TBD)	
PACKAGE (REFERENCE ONLY)	
EMC/ESD LEVEL (REFERENCE ONLY)	
MSL LEVEL/STORAGE CONDITION (REFERENCE ONLY)	
	UIDELINE TO PERFORM SMT WITH MODULE

EXECUTIVE SUMMARY

The WM-BN-BM-26_A module is one of the product families in USI's product offering, targeting for system integration requiring a smaller form factor. It also provides the standard migration to high data rate to USI's current SIP customers.

The purpose of this document is defined the product specification for 802.11b/g/n Wi-Fi with BT4.0 SIP module WM-BN-BM-26_A. All the data in this document is based on Cypress 43438 datasheet and other documents provided from Cypress. The data will be updated after implementing the measurement of the module.

This product is designated for using in embedded applications mainly in the mobile device, which required small size and high data rate wireless connectivity. The application such as, Wireless PDA, slim type Notebook, Media Adapter, Barcode scanner, mini-Printer, VoIP phone, Data storage device could be the potential application for wireless application.

1 BLOCK DIAGRAM

The module is designed based on Cypress 43438 chipset solution. For the WLAN section, two alternative host interface option are included: a SDIO v2.0 interface, which can operate in 4b, 1b or gSPI modes. An independent, high-speed UART is provided for the Bluetooth host interface.

A brief block diagram of the WM-BN-BM-26_A module is depicted as below figure.



WM-BN-BM-26_A Module with packaging

- Evaluation kits (with SDIO/SPI/HSIC/UART interface)
- Software utility which supporting customer for integration, performance test and homologation. Capable of testing, loading (firmware) and configuring (MAC, CIS) for the WM-BN-BM-26_A module.
- Unit Test / Qualification report
- Product Specifications.
- Agency certification pre-test report base on adapter boards

3 REFERENCE DOCUMENTS

C.I.S.P.R. Pub. 22	"Limits and methods of measurement of radio interference characteristics of information technology equipment." International Special Committee on Radio Interference (C.I.S.P.R.), Third Edition, 1997.
CB Bulletin No. 96A	"Adherence to IEC Standards: "Requirements for IEC 950, 2 nd Edition and Amendments 1 (1991), 2(1993), 3 (1995) and 4(1996). Product Categories: Meas, Med, Off, Tron." IEC System for Conformity Testing to Standards for Safety of Electrical Equipment (IECEE), April 2000.
CFR 47, Part 15-B	"Unintentional Radiators". Title 47 of the Code of Federal Regulations, Part 15, FCC Rules, Radio Frequency Devices, Subpart B.
CFR 47, Part 15-C	"Intentional Radiators". Title 47 of the Code of Federal Regulations, Part 15, FCC Rules, Subpart C. URL: http://www.access.gpo.gov/nara/cfr/waisidx 98/47cfr15 98.html
CSA C22.2 No. 950-95	"Safety of Information Technology Equipment including Electrical Business Equipment, Third Edition." Canadian Standards Association, 1995, including revised pages through July 1997.
EN 60 950	"Safety of Information Technology Equipment Including Electrical Business Equipment." European Committee for Electrotechnical Standardization (CENELEC), 1996, (IEC 950, Second Edition, including Amendment 1, 2, 3 and 4).
IEC 950	"Safety of Information Technology Equipment Including Electrical Business Equipment." European Committee for Electrotechnical Standardization, Intentional Electrotechnical Commission. 1991, Second Edition, including Amendments 1, 2, 3, and 4.
IEEE 802.11	"Wireless LAN Medium Access Control (MAC) And Physical Layer (PHY) Specifications," Institute of Electrical and Electronics Engineers. 2012.
C	

4 TECHNICAL SPECIFICATION

4.1 ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Conditions	Min	Мах	Unit
VBAT	Main input supply from battery to switcher		-0.5	4.8	V
VDDIO	DC supply voltage for digital I/O		-0.5	3.9	V
ESD	Electro-static discharge voltage	HBM		2	K۷
Ts	Storage temperature		-40	85	Ċ

4.2 RECOMMENDABLE OPERATION CONDITION

4.2.1 TEMPERATURE, HUMIDITY

The WM-BN-BM-26_A module has to withstand the operational requirements as listed in the table below.

Operating Temperature	-20° to 85° Celsius
Specification Temperature	-20° to 70° Celsius
Humidity range	Max 95% Non condensing, relative humidity

The extreme operating ambient temperature can be up to 85degC, but exposure to absolutemaximum-rated conditions may cause performance degradation and affect device reliability.

4.2.2 VOLTAGE

Power supply for the WM-BN-BM-26_A module will be provided by the host via the power pins

Symbol	Parameter	Min	Тур.	Max	Unit
VBAT	DC supply voltage for VBAT	3.2	3.6	3.9	V
	DC supply voltage for digital I/O	1.71	1.8	- 3.63	V
			3.3		

4.2.3 CURRENT CONSUMPTION

VBATT = +3.6V, VDDIO = +3.3V, TA = 25 $^\circ\!\mathrm{C}$, with 50 Ω nominal system impedance.

2.4GHz

	Item	Condition	Typ(VBAT+VDDIO)	Max	Unit
	1Mbps	Continuous Tx @ 14 dBm	290	350	mA
	11Mbps	Continuous Tx @ 14 dBm	290	350	mA
	6Mbps	Continuous Tx @ 12 dBm	280	350	mA
Тх	54Mbps	Continuous Tx @ 12 dBm	230	300	mA
	MCS0 (HT20)	Continuous Tx @ 12 dBm	280	350	mA
	MCS7 (HT20)	Continuous Tx @ 12 dBm	220	300	mA
	BT Class1	Continuous Tx @ 8 dBm	55	70	mA
	BT Class2	Continuous Tx @ 0 dBm	35	70	mA
	1Mbps	Rx sensitivity @ -95 dBm	45	70	mA
	11Mbps	Rx sensitivity @ -88 dBm	45	70	mA
	6Mbps	Rx sensitivity @ -90 dBm	45	70	mA
Rx	54Mbps	Rx sensitivity @ -73 dBm	45	70	mA
	MCS0 (HT20)	Rx sensitivity @ -89 dBm	45	70	mA
	MCS7 (HT20)	Rx sensitivity @-71 dBm	45	70	mA
	BT	Rx sensitivity @ -85 dbm	22	50	mA
Condition		Typ(VBAT/VDDIO)	Max	Unit	
	ВТ	Sleep Mode	5/150	10/200	uA
	WIF	Sleep Mode	7/80	14/100	uA
	Pov	ver off Mode	3/1	7/3	uA

* Note: The Current Consumption will be updated after samples reliability test

4.3 WIRELESS SPECIFICATIONS

The WM-BN-BM-26_A module complies with the following features and standards;

Features	Description
WLAN Standards	IEEE 802 Part 11b/g/n (802.11b/g/n)
Bluetooth	Bluetooth [™] 4.1 compliance
Antenna Port	Support Single-Band Antenna Shared between Wi-Fi and BT
Frequency Band	2.4 to 2.497GHz (1 to 14 channels)

4.4 RADIO SPECIFICATIONS 802.11B/G/N

The RF performance of WM-BN-BM-26_A is given as follows. Condition: VBAT= 3.6V, VDDIO=3.3V at 25° C

4.4.1 802.11B TRANSMIT

Item	Condition	Min.	Typ. [*] ℃	Max. *d	Unit
Target Output Power Level ^{*b}	1~11Mbps	-	14	17	dBm
Transmit center frequency tolerance*		-25	-	25	ppm
	@+/- 1 1MHz	-	-	-30 ^{*a}	dBr
	@+/-22MHz	-	-	-50 ^{*a}	dBr

* Note: a. Refer to IEEE802.11 specification.

b. Output power tolerance is +/- 2dB

c. Based on the test result at room temperature and typical voltage.

d. Based on the test result at the corner temperature and voltage operating.

4.4.2 802.11G TRANSMIT

Item	Condition	Min.	Typ. [*] ℃	Max. ^{*d}	Unit
Target Output Power Level ^{⁵b}	6~54Mbps	-	12	15	dBm
Transmit center frequency tolerance ^{*a}		-25	-	25	ppm
Transmit Madulation Assurably (E)/M)	54Mbps		-	-25 ^{*a}	dB
	6Mbps		-	15 25 -25 ^{*a} -5 ^{*a} -20 ^{*a} -28 ^{*a} -40 ^{*a}	dB
	@ +/-11MHz			-20 ^{*a}	dBr
Transmit Spectral Mask	@ +/-20MHz		-	- 28 ^{*a}	dBr
	@ +/-30MHz			-40 ^{*a}	dBr

* Note: a. Refer to IEEE802.11 specification.

- b. Output power tolerance is +/- 2dB
- c. Based on the test result at room temperature and typical voltage.
- d. Based on the test result at the corner temperature and voltage operating.

4.4.3 802.11N TRANSMIT – HT20

Item	Condition	Min.	Typ.*c	Max. ^{*d}	Unit
Target Output Power Level ^{*b}	MCS0 ~ MCS7	-	12	14	dBm
Transmit Center Frequency Tolerance		-25	-	25	ppm
Transmit Modulation Accuracy (EVM)	MCS7	-	-	-27 ^{*a}	dB
	MCS0	-	-	-5 ^{*a}	dB
	@ +/-11MHz	-	-	-20 ^{*a}	dBr
Transmit Spectral Mask	@ +/-20MHz	-	-	-28 ^{*a}	dBr
	@ +/-30MHz	-	-	-45 ^{*a}	dBr

*Note: a. Refer to IEEE802.11 specification.

b. Output power tolerance is +/- 2dB.

c. Based on the test result at room temperature and typical voltage.

d. Based on the test result at the corner temperature and voltage operating.

4.4.4 802.11B RECEIVER

Item	Condition	Min.	Typ. ^{*b}	Max. *c	Unit
Receiver Minimum Input Level Sensitivity (PER< 8 %)	11Mbps	-89	-88	-76 ^{*a}	dBm
	1Mbps	-96	-95	-82	dBm
Receiver Maximum Input Level	11Mbps	-10 ^{*a}	-	-	dBm
Sensitivity (PER< 8 %)	1Mbps	-10 ^{*a}	-		dBm

* Note: a. Refer to IEEE802.11 specification.

- b. Based on the test result at room temperature and typical voltage.
- c. Based on the test result at the corner temperature and voltage operating

4.4.5 802.11G RECEIVER

Item	Condition	Min.	Typ. ^{*b}	Max. *c	Unit
Receiver Input Level Sensitivity	54Mb <mark>ps</mark>	-75	-74	-65 ^{*a}	dBm
(PER<10%)	6Mbps 🕂	-90	-89	-82 ^{*a}	dBm
Receiver Maximum Input Level	54Mbps	- 20 ^{*a}	-	-	dBm
(PER<10%)	6Mbps	-20 ^{*a}	-	-	dBm

* Note: a. Refer to IEEE802.11 specification.

- b. Based on the test result at room temperature and typical voltage.
- c. Based on the test result at the corner temperature and voltage operating.

4.4.6 802,11N RECEIVER

Item	Condition	Min.	Typ. ^{*b}	Max. *c	Unit
2.4GHz – HT20 Receiver Input Level Sensitivity	MCS7	-72	-71	-64 ^{*a}	dBm
(PER<10%)	MCS0	-90	-89	-82 ^{*a}	dBm
2.4GHz – HT20 Receiver Maximum Input Level	MCS7	-20 ^{*a}	-	-	dBm
(PER<10%)	MCS0	-20 ^{*a}	-	-	dBm

* Note: a. Refer to IEEE802.11 specification.

- b. Based on the test result at room temperature and typical voltage.
- c. Based on the test result at the corner temperature and voltage operating.

4.5 RADIO SPECIFICATIONS 802.15 BLUETOOTH

The Radio specification is compliant with the Bluetooth [™]2.1 + EDR specification

Features	Description
Frequency Band	2400 MHz ~ 2483.5 MHz
Number of Channels	79 channels
Modulation	FHSS (Frequency Hopping Spread Spectrum), GFSK, DPSK
Antenna Port	Single Antenna for Wi-Fi and BT

The RF performance of WM-BN-BM-26_A is given as follows. Condition: VBAT= 3.6V, VDDIO=3.3V at 25 $^\circ\!C$

4.6 BLUETOOTH RADIO CHARACTERISTICS

Parameter	Conditions	Min.	Typ. ^{*b}	Max. *c	Unit		
Basic Rate			\mathbf{b}				
Output Power	Average Power 🛛 🖊	0	6	20	dBm		
Frequency Range ^{*a}		2400	-	2483.5	MHz		
Sensitivity (BER)	BER ≦0.1%		-90	-70 ^{*a}	dBm		
Maximum Input Level	BER ≦0.1%	-	-	-20 ^{*a}	dBm		
EDR							
Deletive Dever ^{*a}	π/4-DQPSK	-4.0	-1	1.0	dBm		
Relative Power	8DPSK	-4.0	-1	1.0	dBm		
	π/4-DQPSK BER ≦0.01%	-	-85	-70 ^{*a}	dBm		
	8D PSK BER ≦0.01%	-	-85	-70 ^{*a}	dBm		
	π/4-DQPSK BER ≦0.1%	-	-	-20 ^{*a}	dBm		
	8DPSK BER ≦0.1%	-	-	-20 ^{*a}	dBm		
BLE							
BLE Output Power	Average Power	-20	4	10	dBm		
BLE Sensitivity (PER)	PER	-94	-90	-70 ^{*a}	dBm		
BLE Maximum Input Level	PER ≦30.8%	-	-	-10 ^{*a}	dBm		

* Note: a. Refer to Bluetooth specification.

b. Based on the test result at room temperature and typical voltage.

c. Based on the test result at the corner temperature and voltage operating.



4.8 TIMING DIAGRAM OF INTERFACE

4.8.1 CONTROL SIGNAL TIMING DIAGRAMS

Power-up timing for WLAN ON, BT ON *

VBAT	90% of VH
VDDIO	
WL_REG_ON BT_REG_ON 	~ 2 Sleep cycles
	WM-BN-BM-26_A power-up timing for WLAN ON, BT ON
	autour version, version,
Powe	r-up timing for WLAN OFF, BT OFF *
Powe	r-up timing for WLAN OFF, BT OFF *
Powe	r-up timing for WLAN OFF, BT OFF *
22.768 Powe	r-up timing for WLAN OFF, BT OFF *
Powe	r-up timing for WLAN OFF, BT OFF *
Powe 32.768 F VBAT VDOIO	r-up timing for WLAN OFF, BT OFF *

WM-BN-BM-26_A power-up timing for WLAN OFF, BT OFF

32.768 kHz Sleep Clock VBAT 90% of VH VDDIO ~ 2 Sleep cycles WL_REG_ON BT_REG_ON WM-BN-BM-26_A power-up timing for WLAN ON, BT OFF Power-up timing for WLAN OFF, BT ON 32.768 kHz Sleep Clock VBAT 90% of VH VDDIO ~ 2 Sleep cycles WL_REG_ON BT_REG_ON

Power-up timing for WLAN ON, BT OFF *

WM-BN-BM-26_A power-up timing for WLAN OFF, BT ON

*Note:

- VBAT should not raise 10%–90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO.
- VDDIO should NOT be present first or be held high before VBAT is high.

4.8.2 UART TIMING

The WM-BN-BM-26_A shares a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps.



Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	-	0.5	Bit periods



WM-BN-BM-26_A WLAN section provide support for SDIO version 2.0.

Note:

 Per Section 6 of the SDIO specification, pull-ups in the 10 k to 100 k range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pullups



SDIO timing in default mode

SDIO Bus Timing Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimu	m VIH and m	aximum VIL ^b)	8		
Frequency – Data Transfer mode	fPP	0		25	MHz
Frequency – Identification mode	fOD	0		400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	<u> </u>		10	ns
Clock low time	tTHL	-	— 3	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	 2		ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time - Identification mode	tODLY	0		50	ns

a. Timing is based on $CL \le 40 pF$ load on CMD and Data.

b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.



SDIO timing in High-Speed Mode

SDIO Bus Timing Parameters (High-Speed Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum	VIH and ma	ximum VIL ^b)	9		
Frequency – Data Transfer Mode	fPP	0	-	50	MHz
Frequency – Identification Mode	fOD	0		400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7		-	ns
Clock rise time	tTLH			3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	-	-	ns
Input hold Time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5			ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

4.8.4 PCM TIMING

The PCM Interface on the WM-BN-BM-26_A can connect to linear PCM Codec devices in master or slave mode. In master mode, the WM-BN-BM-26_A generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the WM-BN-BM-26_A.



Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock HIGH	41	-	-	ns
3	PCM bit clock LOW	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns





Short Frame Sync, Slave Mode

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock HIGH	41	-	-	ns
3	PCM bit clock LOW	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns







Long Frame Sync, Master Mode

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock HIGH	41	-	-	ns
3	PCM bit clock LOW	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM OUT becoming high impedance	0	-	25	ns







Long Frame Sync, Slave Mode

			´ 🛕 🖤		
Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	_	12	MHz
2	PCM bit clock HIGH	41	-	-	ns
3	PCM bit clock LOW	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns







Short Frame Sync, Burst Mode

Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock HIGH	20.8	-	-	ns
3	PCM bit clock LOW	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns





Ref No.	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock HIGH	20.8	-	-	ns
3	PCM bit clock LOW	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

4.9 FREQUENCY REFERENCES

4.9.1 EXTERNAL 32.768KHZ LOW-POWER OSCILLATOR

The WM-BN-BM-26_A uses a secondary low frequency clock for low-power-mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz \pm 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed below.

External 32.768 kHz Sleep Clock Specifications

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30-70	%
Input signal amplitude	200–3300	mV, p-p
Signal type Square-wave or sine-wave		-
Input impedance ^a	>100k	Ω
	<5	pF
Clock jitter (during initial start-up)	<10,000	ppm

a. When power is applied or switched off.



4.10 DIMENSIONS, WEIGHT AND MOUNTING

The following paragraphs provide the requirements for the size, weight and mounting of the WM-BN-BM-26_A SiP module.

4.10.1 DIMENSION & MODEL CODE

The size and thickness of the WM-BN-BM-26_A module is "9.5 mm \pm 0.1"(L) x "15 mm \pm 0.1(W)" x "1.8 mm" (Max.)(H), with metal shielding and the maximum height in antenna area is 2.0mm.





Dimensio	ons						(unit:mm)
Mark	Dimensions	Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	15+/-0.1	W	9.5+/-0.1	Т	Max1.80	T1	Max2.00
a1	1.00+/-0.1	a2	0.35+/-0.1	c1	0.65+/-0.1	c2	0.65+/-0.1
a3	0.35+/-0.1	a4	0.65+/-0.1	b2	1.42+/-0.2	b3	2.02+/-0.2
c3	1.00+/-0.1	b1	0.15+/-0.1	b6	2.42+/-0.2	e4	2.62+/-0.2
b4	0.15+/-0.1	b5	0.15+/-0.1	e3	1.02+/-0.2		
e1	0.7+/-0.1	e2	2.22+/-0.2				

5 LEGAL, REGULATORY & OTHER TECHNICAL CONSTRAINTS

The WM-BN-BM-26_A module is pre-tested to ensure that all requirements compliant with FCC and CE.

Customers could leverage the print antenna on board or external antenna to do the final certification for the flexible way.





Top View

Pin#	Pin Name	Туре	Description		
RF P	ort				
3	WLAN_BT_ANT	I/O	WLAN/BT Transmit/Receive Antenna Port		
WLA	N SDIO Interface (level r	referre	d by VDDIO)		
8	WL_SDIO_CLK		SDIO Bus clock input		
12	WL_SDIO_D0	I/O	SDIO Bus data line 0		
10	WL_SDIO_D2	I/O	SDIO Bus data line 2		
11	WL_SDIO_CMD	I/O	SDIO Bus command line		
14	WL_SDIO_D1	I/O	SDIO Bus data line 1		
13	WL_SDIO_D3	I/O	SDIO Bus data line 3		
Bluet	ooth UART Interface (le	vel ret	ferred by VDDIO)		
33	BT_UART_CTS_N	I	Bluetooth UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.		
35	BT_UART_RXD	Ι	Bluetooth UART serial input. Serial data input for the HCLUART Interface.		
32	BT_UART_RTS_N	0	Bluetooth UART request-to-send. Active-low request-to-send signal for the HCI UART interface.		
34	BT_UART_TXD	0	Bluetooth UART serial output. Serial data output for the HCI UART Interface.		
Bluet	ooth PCM Interface (lev	el refe	erred by VDDIO)		
28	BT_PCM_CLK	I/O	PGM clock can be master (output) or slave (input).		
31	BT_PCM_IN		PCM data input.		
29	BT_PCM_SYNC	I/O	PCM sync signal can be master (output) or slave (input).		
30	BT_PCM_OUT	Q	PCM data output.		
Refer	rence Clock				
25	LPO_IN	<u> </u>	External sleep clock input (32.768 kHz)		
GPIO	and Control Signal (lev	el refe	rred by VDDIO)		
17	WL_GPIO_1	1/0	This pin can be programmed by software to be a GPIO		
6		I/O	This pin can be programmed by software to be a GPIO		
16	WL_HOST_WAKE (WL_GPIO_0)	I/O	This pin can be programmed by software to be a GPIO or a WLAN_HOST_WAKE output indicating that host wake-up should be performed.		
<mark>_3</mark> 8	BT_HOST_WAKE	0	Bluetooth HOST_WAKE		
37	BT_DEV_WAKE	I	Bluetooth DEV_WAKE		
24	BT_REG_ON	Ι	Used by PMU to power up or power down the internal CYW43438 regulators used by the BT/FM section. This pin has an internal 200kOhm pull-down resistor that is enabled by default. It can be disabled through programming.		
18	WL_REG_ON	I	Used by PMU to power up or power down the internal CYW43438 regulators used by the WLAN section. This pin has an internal 200kOhm pull-down resistor that is		

Pin#	Pin Name	Туре	Description
			enabled by default.
			It can be disabled through programming.
Power	r Supplies	•	
21	VBAT		Battery supply input
22	VBAT	I	Battery supply input
19	VDDIO		Digital I/O supply input
Groun	nd		
1	GND	-	Ground
2	GND	-	Ground
4	GND	-	Ground
5	GND	-	Ground
7	GND	-	Ground
9	GND	-	Ground
15	GND	-	Ground
20	GND	-	Ground
23	GND	-	Ground
26	GND	-	Ground
27	GND	-	Ground
36	GND	-	Ground
39	GND	-	Ground
40	GND	-	Ground
41~50) GND	-	Ground
H1~H	9 GND	-	Ground

7 GUIDELINE TO PERFORM SMT WITH MODULE

7.1 PCB FOOTPRINT RECOMMENDATION





Top View



7.2 RECOMMENDED REFLOW PROFILE

8 PACKAGE AND STORAGE CONDITION (TBD)

8.1 PACKAGE (REFERENCE ONLY)



8.2 EMC/ESD LEVEL (REFERENCE ONL)

According to FCC and CE standard Surface Resistivity: Interior: $10^9 \sim 10^{11}\Omega$ /SQUARE EXTERIOR: $10^8 \sim 10^{12}\Omega$ /SQUARE Dimension: 475^{420} mm Tolerance:+5,0mm Color: Background : Gray Text : Red

8.3 MSL LEVEL/STORAGE CONDITION (REFERENCE ONLY)

