Product Data Sheet
Of USI
WM-BAC-BM-28
SiP Module

802.11a/b/g/n/ac BM-28 with BT4.2 SiP Module V3.4

Introduction

The 802.11a/b/g/n/ac with BT4.2 Sip module which refers as “WM-BAC-BM-28 SiP module” is a small size module based on LGA package that provides full function of 802.11a/b/g/n/ac 1x1 spatial stream with Bluetooth 4.2 in a tiny module via 72 pins LGA Footprint.

This multi-functionality and board to board physical interface provides SDIO v3.0 for Wi-Fi and UART for Bluetooth.

The small size & low profile physical design make it easier for system design to enable high performance wireless connectivity without space constrain. The low power consumption and excellent radio performance make it the best solution for OEM customers who require embedded 802.11a/b/g/n/ac dual-band Wi-Fi features, such as, Wireless PDA, Smart phone, MP3, PMP, slim type Notebook, VoIP phone etc.

The module is based on CYW43455 Wi-Fi chipset. The Radio architecture & high integration MAC/BB chip provide excellent sensitivity. The module is designed as dual-antenna for Wi-Fi and a single 2.4GHz antenna dedicated for Bluetooth only.

In addition to WPA, WPA2 and TKIP, AES is supported to provide the latest security requirement on your network.

For the software and driver development, USI provides extensive technical document and reference software code for the system integration.

Hardware evaluation kit and development utilities will be released base on listed OS and processors to OEM customers.

Features

- Lead Free design which supporting Green design requirement, RoHS Compliance, and halogen-free.
- Supports dual-antenna for Wi-Fi
- Supports a dedicated bluetooth antenna
- Excellent Sensitivity. Good Isolation between Wi-Fi and CDMA Small size suitable for low volume system integration.Low power consumption & excellent power management performance extend battery life.
- WiFi Only and WAN for LTE two SKUs for worldwide market.
- Easy for integration into mobile and handheld device with flexible system configuration and antenna design.

***This document is subject to change without notice.**

802.11a/b/g/n/ac BM-28 with BT4.2 SiP Module V3.4

Change Sheet			
Rev.	**Date**	**Description of change** **Change(s)**	**Prepared by**
1.0	2016.11.09	Preliminary Release	Cren
1.1	2016.11.17	Add ch 144 for 5G in Page 12	Cren
2.0	2017.02.22	1. Update BT to 4.2 2. Update some current consumption values	Cren
3.0	2017.04.18	Correct some typos	Cren
3.1	2017.05.02	Update spec.	Cren
3.2	2017.09.25	Use two blocks For BPF sku and without Filter sku.	Cren
3.3	2017.01.10	1. Modify ESD HBM to 1kV Max. 2. Update BT and WFi sleep current	Cren
3.4	2017.01.17	Remove BPF sku from document	Cren

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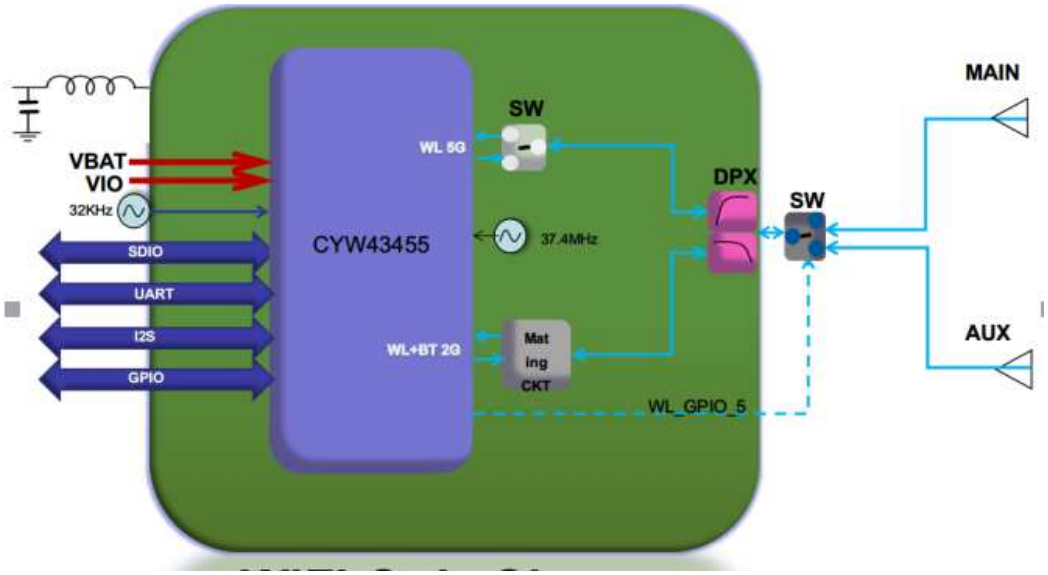
1. EXECUTIVE SUMMARY

This document specifies the requirement for a WiFi 802.11a/b/g/n/ac with BT4.2 SIP module (called "WM-BAC-BM-28")proposed for next generation USI cutting edge SiP module. The proposed module will use CYW 43455 chip set integrated with LNA, switch, diplexer and harmonic filter for small form factor and optimum performance. Integration of diplexers and filter(s) will ensure maximum power flatness and optimum VSWR. The module will perform with all legacy hardware having data rates as low as 1 Mbps.
This module also supports concurrent operation of Bluetooth (Version 4.2) for wireless connectivity during browsing or other device applications. Along with both standard and high speed (HS) Bluetooth data rates, Bluetooth low energy modes are also supported.

This product is designated for use in embedded applications mainly in the mobile device, which required small size and high data rate wireless connectivity. The application such as, Wireless PDA, slim type Notebook, Media Adapter, Barcode scanner, mini-Printer, VoIP phone, Data storage device could be the potential application for wireless application.

2. BLOCK DIAGRAM

The module uses the CYW 43455 chipset as its core solution. For the WiFi side there are two alternative host interface options 1) SDIO v3.0,which can operate in 4bit or 1bit, The Bluetooth side is controlled via an independent, high speed UART host interface.



At the heart of the module is the CYW43455 chipset. This chipset has internal power amplifiers (iPAs) so only one TR switche at 5G is needed to route signals to and from the 43455 device.
The 2G and 5G signals are fed to the antenna (dual band) using a diplexer filter.

The signal interfaces are shown on the left side of the block diagram and include SDIO 3.0, and BT UART interfaces. For efficiency the switching inductor and capacitor are external to the module as shown. A 37.4 MHz main clock crystal is internal to the module for frequency stability.

3. DELIVERABLES

The following products and software will be part of the product.

- BM-28 SiP Module with packaging
- Evaluation kits (with SDIO interface)
- Software utility which supporting customer for integration, performance test, and homologation. Capable of testing, loading (firmware) and configuring (MAC, CIS) for the module.
- Unit Test / Qualification report
- Product Specifications.
- Agency certification pre-test report base on adapter boards

4. REFERENCE DOCUMENTS

C.I.S.P.R. Pub. 22	"Limits and methods of measurement of radio interference characteristics of information technology equipment." International Special Committee on Radio Interference (C.I.S.P.R.), Third Edition, 1997.
CB Bulletin No. 96A	"Adherence to IEC Standards: "Requirements for IEC 950, 2nd Edition and Amendments 1 (1991), 2(1993), 3 (1995) and 4(1996). Product Categories: Meas, Med, Off, Tron." IEC System for Conformity Testing to Standards for Safety of Electrical Equipment (IECEE), April 2000.
CFR 47, Part 15-B	"Unintentional Radiators". Title 47 of the Code of Federal Regulations, Part 15, FCC Rules, Radio Frequency Devices, Subpart B.
CFR 47, Part 15-C	"Intentional Radiators". Title 47 of the Code of Federal Regulations, Part 15, FCC Rules, Subpart C. URL: http://www.access.gpo.gov/nara/cfr/waisidx_98/47cfr15_98.html
CSA C22.2 No. 950-95	"Safety of Information Technology Equipment including Electrical Business Equipment, Third Edition." Canadian Standards Association, 1995, including revised pages through July 1997.
EN 60 950	"Safety of Information Technology Equipment Including Electrical Business Equipment." European Committee for Electrotechnical Standardization (CENELEC), 1996, (IEC 950, Second Edition, including Amendment 1, 2, 3 and 4).
IEC 950	"Safety of Information Technology Equipment Including Electrical Business Equipment." European Committee for Electrotechnical Standardization, Intentional Electrotechnical Commission. 1991, Second Edition, including Amendments 1, 2, 3, and 4.
IEEE 802.11	"Wireless LAN Medium Access Control (MAC) And Physical Layer (PHY) Specifications." Institute of Electrical and Electronics Engineers. 1999.

5. TECHNICAL SPECIFICATION

5.1 ABSOLUTE MAXIMUM RATINGs

*1)

Symbol	Parameter	Conditions	Min	Max	Unit
VBAT_	Main input supply from battery to switcher		0	5.0	V
VDDIO	DC supply voltage for I/O		0	3.9	V
ESD	Electro-static discharge voltage	HBM		1.0	KV
Ts	Storage temperature		-40	85	℃

*1) Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

5.2 RECOMMENDABLE OPERATION CONDITION

5.2.1 TEMPERATURE, HUMIDITY

Operating Temperature *2)	-20°to 85°C
Humidity range	Max 85% Non condensing, relative humidity

*2) The max. Operating ambient temperature rang can be 85°C, but exposure to absolute-maximum-rated conditions may cause performance degradation and affect device reliability.

5.2.2 VOLTAGE

Symbol	Parameter	Min	Typ	Max	Unit
VBAT / VBAT_SR	DC supply for VBAT *3,4)	3.2	3.6	4.8	V
VIO	DC supply voltage for I/O	1.62	-	3.63	V

*3) Functionality is guaranteed but the specifications require the derating at over-temperatures, over-voltage condition.

*4) Best RF performance specified in the data sheet, is suggested to be 3.4V ~ 4.8V

5.2.3 Digital I/O Requirement

		Value			
I/O pins	Symbol	Min	Typical	Max	Unit
VIO=1.8V					
Input high voltage	VIH	0.65xVIO	-	-	V
Input low voltage	VIL	-	-	0.35xVIO	V
Output high voltage@2mA	VOH	VIO-0.45	-	-	V

Output low voltage@2mA	VOL	-	-	0.45	V
VIO=3.3V					
Input high voltage	VIH	2.00	-	-	V
Input low voltage	VIL	-	-	0.80	V
Output high voltage@2mA	VOH	VIO-0.4	-	-	V
Output low voltage@2mA	VOL	-	-	0.40	V

5.3 CURRENT CONSUMPTION

The RF characteristics are tested under nominal supply voltage and room temperature conditions.

WLAN MAX. Power Consumption (25C, Vbat 3.6V) 2.4GHz					
		Output Power	VBAT = 3.6V	VDDIO = 3.3V	Units
OFF	WL_REG_ON = low BT_REG_ON = low		6	-	uA
Sleep			40		uA
Continuous Rx mode 1 Mbps			80		mA
Continuous Rx mode 11 Mbps			82		mA
Continuous Rx mode 6Mbps			83		mA
Continuous Rx mode 54Mbps			85		mA
Continuous Rx mode MCS0– HT20			83		mA
Continuous Rx mode MCS7 – HT20			85		mA
Continuous Rx mode MCS0 – VHT20			85		mA
Continuous Rx mode MCS8 – VHT20			88		mA
Continuous Tx mode 1 Mbps		17.5	423		mA
Continuous Tx mode 11 Mbps		17.5	425		mA
Continuous Tx mode 6 Mbps		15	379		mA
Continuous Tx mode 54 Mbps		15	281		mA
Continuous Tx mode MCS0 – HT20		15	369		mA
Continuous Tx mode MCS7 – HT20		15	273		mA
Continuous Tx mode MCS0 –VHT20		14	360		mA
Continuous Tx mode MCS8 –VHT20		14	258		mA

WLAN MAX. Power Consumption (25C, Vbat 3.6V) 5GHz					
Parameter		Output Power	VBAT = 3.6V	VDDIO = 3.3V	Units
OFF	WL_REG_ON = low BT_REG_ON = low		6	-	uA
Continuous Rx mode 6Mbps			99		mA
Continuous Rx mode 54Mbps			99		mA
Continuous Rx mode MCS0 HT20			99		mA
Continuous Rx mode MCS7 HT20			99		mA
Continuous Rx mode MCS0 HT40			106		mA
Continuous Rx mode MCS7 HT40			106		mA
Continuous Rx mode MCS0 VHT20			99		mA
Continuous Rx mode MCS8 VHT20			99		mA
Continuous Rx mode MCS0 VHT40			106		mA

Continuous Rx mode MCS9 VHT40		**106**		**mA**
Continuous Rx mode MCS0 VHT80		**135**		
Continuous Rx mode MCS9 VHT80		**135**		**mA**
Continuous Tx mode 6 Mbps	**15**	**371**		**mA**
Continuous Tx mode 54 Mbps	**15**	**286**		**mA**
Continuous Tx mode MCS0 HT20	**15**	**366**		**mA**
Continuous Tx mode MCS7 HT20	**15**	**278**		**mA**
Continuous Tx mode MCS0 HT40	**15**	**360**		**mA**
Continuous Tx mode MCS7 HT40	**15**	**253**		**mA**
Continuous Tx mode MCS0 VHT20	**14**	**357**		**mA**
Continuous Tx mode MCS8 VHT20	**14**	**262**		**mA**
Continuous Tx mode MCS0 VHT40	**13**	**341**		**mA**
Continuous Tx mode MCS9 VHT40	**13**	**233**		**mA**
Continuous Tx mode MCS0 VHT80	**12**	**332**		**mA**
Continuous Tx mode MCS9 VHT80	**12**	**229**		**mA**

BT Power Consumption@10dBm output (25C, Vbat 3.6V)		
Operating Mode	**Typical**	**Units**
Continuous Rx Power	63	mA
Sleep mode	41	uA
DM1/DH1	60	mA
DM3/DH3	65	mA
DM5/DH5	65	mA

*** Note: the current consumption data will be updated after samples verification test.**

Note:

- The WLAN core is in reset (WL_REG_ON = low) for all measurements.
- The BT current consumption numbers are measured based on GFSK Tx output power = 10dBm

5.4 WIFI RF TRANSMITTER SPECIFICATION

VBAT = 3.6V, ambient temperature = 25 ℃ ,
Output power @module RF antenna port

5.4.1 TARGET POWER THAT MEET SPECTRUM MASK AND EVM COMPLIANCE

2.4GH z TX power specification							
Std	**Mod**	**Rate**	**BW**	**Channel**	**Spec (TYP.)**	**Units**	Tol. **(dB)**
11b	CCK, DSSS	1-11 Mbps	20 MHz	1-13	17.5	dBm	+/- 2.0
11g	OFDM	6 - 54 Mbps	20 MHz	1-13	15	dBm	+/- 2.0
11n	OFDM	MCS 0-7	20 MHz	1-13	15	dBm	+/- 2.0
11ac	OFDM	MCS 0-8	20 MHz	1-13	14	dBm	+/- 2.0
5GH z TX power specification							
Std	**Mod**	**Rate**	**BW**	**Channel**	**Spec (TYP.)**	**Units**	Tol. **(dB)**
11a	OFDM	6 - 54 Mbps	20 MHz	36-48 52-64 100-144 149-165	15	dBm	+/- 2.0
11n	OFDM	MCS 0-7	20 MHz	36-48 52-64 100-144 149-165	15	dBm	+/- 2.0
11n	OFDM	MCS 0- 7	40 MHz	36-48 52-64 100-144 149-165	15	dBm	+/- 2.0
11ac	OFDM	MCS 0- 8	20 MHz	36-48 52-64 100-144 149-165	14	dBm	+/- 2.0
11ac	OFDM	MCS 0- 9	40 MHz	36-48 52-64 100-144 149-165	13	dBm	+/- 2.0
11ac	OFDM	MCS 0-9	80MHz	36-48 52-64 100-144 149-165	12	dBm	+/- 2.0

5.4.2 TX SPECTRUM AND EVM AND FREQUENCY ACCUARCY AT NOMINAL OUTPUT POWER

Transmit spectrum mask					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
11b	@ 11MHz	-	-	-30*	dBr
	@22MHz	-	-	-50*	dBr
11a/g	@ 11MHz	-	-	-20*	dBr
	@ 20MHz	-	-	-28*	dBr
	@ 30MHz	-	-	-40*	dBr
11n/ac. HT20	@ 11MHz	-	-	-20*	dBr
	@ 20MHz	-	-	-28*	dBr
	@ 30MHz	-	-	2G: -45* 5G: -40*	dBr
11n/ac, HT40	@ 21MHz	-	-	-20*	dBr
	@ 40MHz	-	-	-28*	dBr
	@ 60MHz	-	-	2G: -45* 5G: -40*	dBr
11ac, VHT80	@ 41MHz	-	-	-20*	dBr
	@ 80MHz	-	-	-28*	dBr
	@ 120MHz	-	-	2G: -45* 5G: -40*	dBr

Transmit modulation accuracy (Error Vector Magnitude)					
Parameter	**Condition**	**Unit**	**Min**	**Typ**	**Max**
11b	1 ~ 11Mbps	dB	-	-	-9.12*
11ag	6 Mbps	dB	-	-	-5 *
	54 Mbps	dB	-	-	-25*
11n	MCS0	dB	-	-	-5 *
	MCS7	dB	-	-	-27*
11ac MCS0	All MCS0	dB	-	-	-5*
11ac MCS7	All MCS7	dB	-	-	-27*
11ac MCS8	All MCS8	dB	-	-	-30*
11ac MCS9	All MCS9	dB	-	-	-32*

Transmit Center Frequency Tolerance For 2G/5G and all Data rates	**Unit**	**Min**	**Typ**	**Max**
	ppm	-20	-	20

* IEEE spec.

5.5 WIFI RF RECEIVER SPECIFICATION

VBAT = 3.6V Ambient temperature = 25 ℃,

5.5.1 2.4GHZ SENSITIVITY

5.5.1.1 2.4 GHz

		Spec.			
Parameter	**Condition**	**Min**	**Typ**	**Max***	**Unit**
RX sensitivity in 802.11b mode					
1Mbps	PER<8%, packet size=1024 bytes		-95	-82	dBm
11Mbps			-87	-76	dBm
RX sensitivity in 802.11g mode					
6Mbps	PER<10%, packet size=1024 bytes	-	-92	-82	dBm
54Mbps		-	-75	-65	dBm
RX sensitivity in 802.11n mode 20 MHz channel spacing for all MCS rates					
MCS0	PER<10%, packet size=1024 bytes		-90	-82	dBm
MCS7			-73	-64	dBm
RX sensitivity in 802.11ac mode 20 MHz channel spacing for all MCS rates					
MCS0	PER<10%, packet size=1024 bytes		-89	-82	dBm
MCS8			-67	-59	dBm
Maximum input level					
802.11b	PER<8%, packet size=1024 byte	-10	-	-	dBm
802.11g	PER<10%, packet size=1024 byte	-20	-	-	dBm
802.11n	PER<10%, packet size=1024 byte	-20	-	-	dBm
802.11ac	PER<10%, packet size=1024 byte	-20	-	-	dBm

* IEEE standard

5.5.2 5GHZ SENSITIVITY

5.5.2.1 5G GHz

		BM-28 Spec			
Parameter	**Condition**	**Min**	**Typ**	**Max***	**Unit**
RX sensitivity in 802.11a mode					
6Mbps	PER<10%, packet size=1024 bytes	-	-92	-82	dBm
54Mbps		-	-75	-65	dBm

RX sensitivity in 802.11n mode – 20 MHz channel					
MCS0	PER<10%, packet size=1024 bytes		-92	-82	dBm
MCS7			-72	-64	dBm
RX sensitivity in 802.11n mode – 40 MHz channel					
MCS0	PER<10%, packet size=1024 bytes		-89	-79	dBm
MCS7			-70	-61	dBm
RX sensitivity in 802.11ac mode – 20 MHz channel					
MCS0	PER<10%, packet size=1024 bytes		-91	-82	dBm
MCS8			-68	-59	dBm
RX sensitivity in 802.11ac mode – 40 MHz channel					
MCS0	PER<10%, packet size=1024 bytes		-89	-79	dBm
MCS9			-64	-54	dBm
RX sensitivity in 802.11ac mode – 80 MHz channel					
MCS0	PER<10%, packet size=1024 bytes		-86	-76	dBm
MCS9			-62	-51	dBm
Maximum input level					
802.11a	PER<10%, packet size=1024 byte	-30	-	-	dBm
802.11n	PER<10%, packet size=1024 byte	-30	-	-	dBm
802.11ac	PER<10%, packet size=1024 byte	-30	-	-	dBm

* IEEE standard

5.6 BLUETOOTH RF CHARACTERISTICS

VBAT = 3.6V
Ambient temperature = 25 ℃

BT BDR Features	Description		
	Min.	Typical	Max.
RF frequency range	2400MHz	-	2483.5MHz
Maximum Receive Level	-	-	-20dBm
Basic rate (GFSK) Tx Power	0dBm	-	20dBm
QPSK Tx Power	0dBm	-	20dBm
8PSK Tx Power	0dBm	-	20dBm
Rx Sensitivity (GFSK, 0.1% BER, 1 Mbps)	-	-90dBm	-70dBm
Rx Sensitivity (π/4 – DQPSK, 0.01% BER, 2 Mbps)	-	-93dBm	-70dBm
Rx Sensitivity (8– DPSK, 0.01% BER, 3Mbps)	-	-87dBm	-70dBm
Modulation characteristics			
Δ f1 $_{Avg.}$	**$140 \leq \Delta f1_{Avg.} \leq 175$**		**KHz**
Δ f2 $_{Max}$	**$\Delta f2_{Max} \geq 115$**		**KHz**
$\Delta f2_{Avg.} / \Delta f1_{Avg.}$	**≥ 0.80**		
Freq Drift DH1	-25KHz	-	+25KHz
Freq Drift DH3	-40KHz	-	+40KHz
Freq Drift DH5	-40KHz	-	+40KHz
Drift Rate **(/50us)**	-20KHZ	-	+20KHz
Initial Carrier Freq Tolerance (ICFT)	-75KHz	+/-30KHz	+75KHz

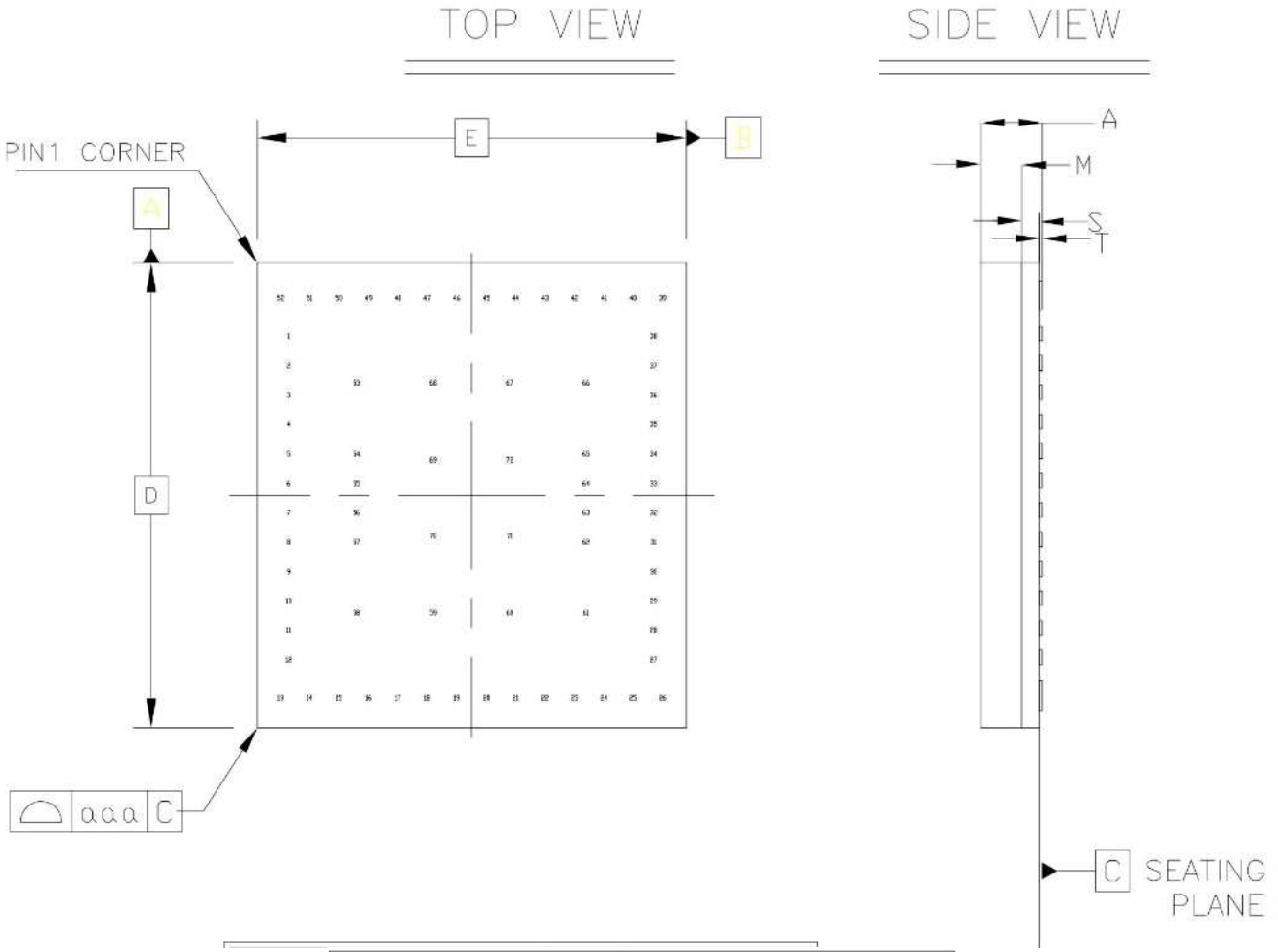
BT Low Energe Features	Description		
	Min.	Typical	Max.
Center Frequency (spacing 2MHz)	2402M	-	2480MHz
Output Power	-20dBm	-	10dBm
Rx Sensitivity	-	-	-70dBm
Modulation characteristics			
$\Delta f1_{Avg.}$	**$225 \leq \Delta f1_{Avg.} \leq 275$**		KHz
$\Delta f2_{MAX}$	**$\Delta f2_{Max} \geq 185$**		KHz
$\Delta f2_{Avg.} / \Delta f1_{Avg.}$	**≥ 0.80**		-
Carrier frequency offset and drift			
Absolute Frequency Offset	**$\lvert f_n - f_{TX} \rvert \leq 150$ KHz** n=0,1,2,⋯,k f_{TX} is the nominal TX frequency		
Carrier Drift – Drift Rate (/50us)	-20KHz	-	+20KHz
Frequency Drift	-50KHz	-	+50KHz

* Recorded over 10 test packets

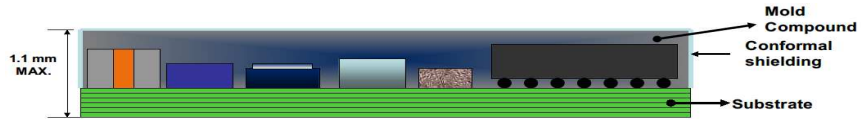
5.7 MECHANICAL DIMENSIONS, WEIGHT AND MOUNTING

The following paragraphs provide the requirements for the size, weight and mounting of the BM-28 SiP Module. The size and thickness of the dual-band WALN module is 7.9mm (L) x 7.3mm (W) x 1.1mm (H). Package type is on LGA.

Figure 1 Module Mechanical Dimension

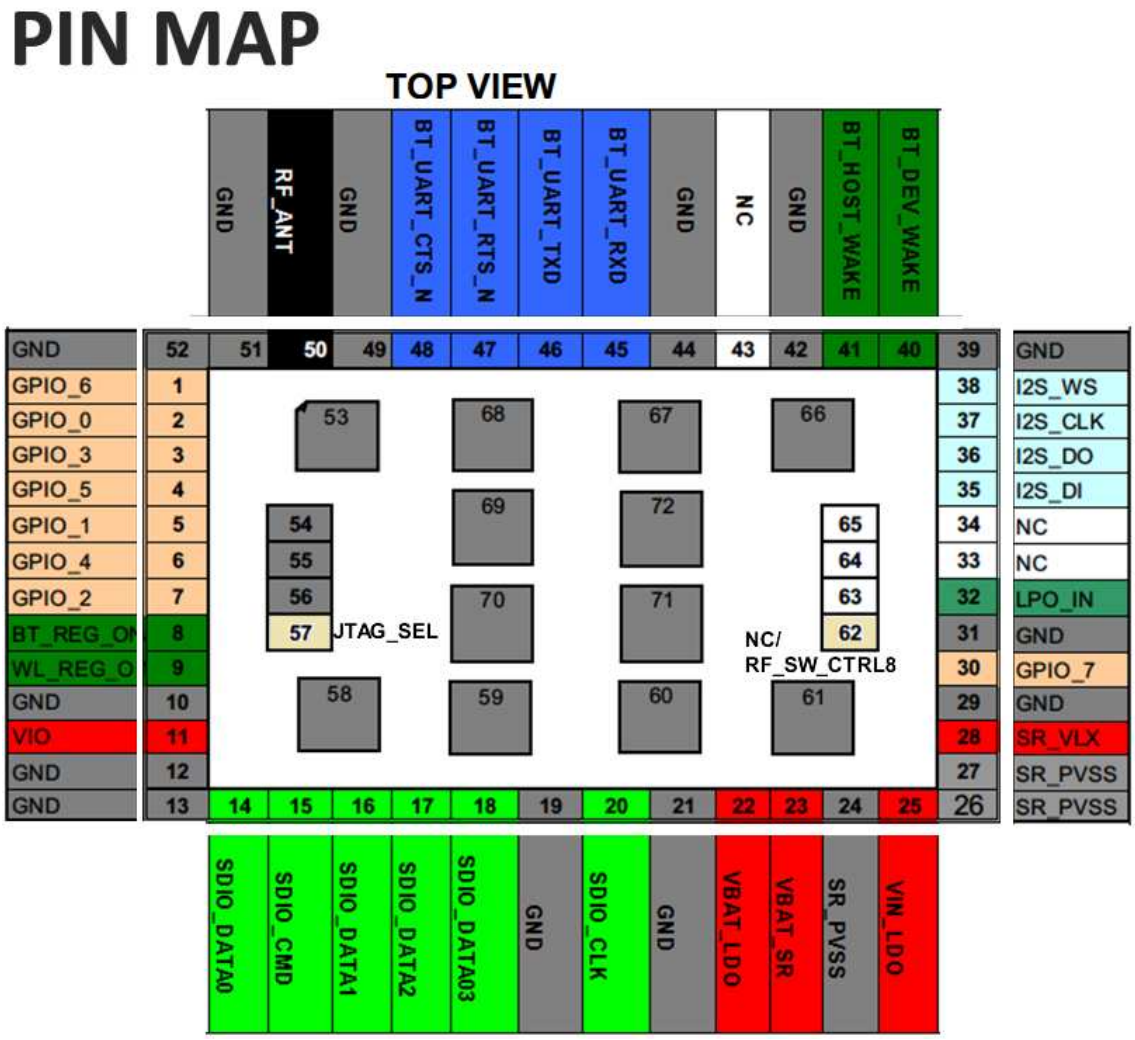


		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :		PIM	---		
Body Size:	X	E		7.300	
	Y	D		7.900	
Ball Pitch :		e		0.500	
Total Thickness :		A	---	---	1.100
Mold Thickness :		M	0.670	0.700	0.730
Substrate Thickness :		S	0.264	0.304	0.344
Bump Thickness :		T	---	---	0.050



6. PIN DEFINITION

6.1 PINS DESCRIPTION



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	GPIO_6	19	GND	37	I2S_CLK	55	GND
2.	GPIO_0	20	SDIO_CLK	38	I2S_WS	56	GND
3	GPIO_3	21	GND	39	GND	57	JTAG_SEL
4	GPIO_5	22	VBAT_LDO	40	BT_DEV_WAKE	58	GND
5	GPIO_1	23	VBAT_SR	41	BT_HOST_WAKE		
6	GPIO_4	24	SR_PVSS	42	GND		
7	GPIO_2	25	VIN_LDO	43	NC	61	GND
8	BT_REG_ON	26	SR_PVSS	44	GND	62	NC / RF_SW_CTRL8
9	WL_REG_ON	27	SR_PVSS	45	BT_UART_RXD	63	NC
10	GND	28	SR_VLX	46	BT_UART_TXD	64	NC
11	VIO	29	GND	47	BT_UART_RTS_N	65	NC
12	GND	30	GPIO_7	48	BT_UART_CTS_N	66	GND
13	GND	31	GND	49	GND	67	GND
14	SDIO_DATA0	32	LPO_IN	50	ANT	68	GND
15	SDIO_CMD	33	NC	51	GND	69	GND
16	SDIO_DATA1	34	NC	52	GND	70	GND
17	SDIO_DATA2	35	I2S_DI	53	GND	71	GND
18	SDIO_DATA3	36	I2S_DO	54	GND	72	GND

<Top View>

Module Pin Assignment (Top View)

The pins definition are as below：

Table 6-1 Module Pin Definitions

No.	Pin name	Type	System	Connection to IC pin name	Description
1	GPIO_6	I/O	WL	GPIO_6	JTAG_SEL=1: GPIO_6 is TRST_L
2	GPIO_0	I/O	WL	GPIO_0	GPIO Programmable Pin
3	GPIO_3	I/O	WL	GPIO_3	JTAG_SEL=1: GPIO_3 is TMS/SWDIO
4	GPIO_5	I/O	WL	GPIO_5	JTAG_SEL=1: GPIO_5 is TDO
5	GPIO_1	I/O	WL	GPIO_1	GPIO Programmable Pin
6	GPIO_4	I/O	WL	GPIO_4	JTAG_SEL=1: GPIO_4 is TDIO
7	GPIO_2	I/O	WL	GPIO_2	JTAG_SEL=1: ·GPIO_2 is TCK/SWCLK
8	BT_REG_ON	I	BT	BT_REG_ON	Used by PMU to power up or power down the internal CYW43455 regulators used by the BT section. Also, when deserted, this pin holds the BT section in reset. This pin has an internal 200k ohm pull-down resistor that is enabled by default. It can be disabled through programming.
9	WL_REG_ON	I	WL	WL_REG_ON	Used by PMU to power up or power down the internal CYW43455 regulators used by the WLAN section. Also, when deserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull-down resistor that is enabled by default. It can be disabled through programming.
10	GND	-	-	-	-
11	VIO	I	-	VDDIO, VDDIO_SD, BT_VDDO	Supply for PMU, BT, WLAN, SDIO.
12	GND	-	-	-	-
13	GND	-	-	-	-
14	SDIO_DATA_0	I/O	WL	SDIO_DATA_0	SDIO data line 0
15	SDIO_CMD	I/O	WL	SDIO_CMD	SDIO command line
16	SDIO_DATA_1	I/O	WL	SDIO_DATA_1	SDIO data line 1
17	SDIO_DATA_2	I/O	WL	SDIO_DATA_2	SDIO data line 2
18	SDIO_DATA_3	I/O	WL	SDIO_DATA_3	SDIO data line 3
19	GND	-	-	-	-
20	SDIO_CLK	I	WL	SDIO_CLK	SDIO clock input
21	GND	-	-	-	-
22	VBAT_LDO	I	-	LDO_VDDBAT5V	Power supply
23	VBAT_SR	I	-	SR_VDDBAT5V	Power supply
24	SR_PVSS	-	-	-	Connect to GND
25	VIN_LDO	I	-	LDO_VDD1P5	LNLDO input
26	SR_PVSS	-	-	-	Connect to GND
27	SR_PVSS	-	-	-	Connect to GND
28	SR_VLX	O	-	SR_VLX	CBuck switching regulator output.
29	GND	-	-	-	-
30	GPIO_7	I/O	WL	GPIO_7	Strapping option for SDIO I/F voltage 1=1.8V (NC) 0=3.3V (Pull down with 10k ohm resister)
31	GND	-	-	-	-
32	LPO_IN	I	-	LPO_IN	External Sleep clock input(32.768kHz)

33	NC	-	-	-	NC
34	NC	-	-	-	NC
35	BT_I2S_DI	I/O	BT	BT_I2S_DI	I2S data input
36	BT_I2S_DO	I/O	BT	BT_I2S_DO	I2S data output
37	BT_I2S_CLK	I/O	BT	BT_I2S_CLK	I2S clock, can be master (output) or slave (input).
38	BT_I2S_WS	I/O	BT	BT_I2S_WS	I2S WS; can be master (output) or slave (input).
39	GND	-	-	-	-
40	BT_DEV_WAKE	I	BT	BT_DEV_WAKE	Bluetooth DEV_WAKE
41	BT_HOST_WAKE	O	BT	BT_HOST_WAKE	Bluetooth HOST_WAKE
42	GND	-	-	-	-
43	NC	-	-	-	NC
44	GND	-	-	-	-
45	BT_UART_RXD	I	BT	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.
46	BT_UART_TXD	O	BT	BT_UART_TXD	UART serial output. Serial data output for the HCI UART interface.
47	BT_UART_RTS	O	BT	BT_UART_RTS_N	UART request – to - send. Active - low request - to-send signal for the HCI UART interface.
48	BT_UART_CTS	I	BT	BT_UART_CTS_N	UART clear – to - send. Active - low clear – to - send signal for the HCI UART interface.
49	GND	-	-	-	-
50	ANT	I/O	-	-	-
51	GND	-	-	-	-
52	GND	-	-	-	-
53	GND	-	-	-	-
54	GND	-	-	-	-
55	GND	-	-	-	-
56	GND	-	-	-	-
57	JTAG_SEL	I/O	-	JTAG_SEL	JTAG select. This pin must be connected to ground if the JTAG/SWD interface is not used. It must be high to select SWD OR JTAG. When JTAG_SEL=1: ·GPIO_2 is TCK/SWCLK ·GPIO_3 is TMS/SWDIO ·GPIO_4 is TDIO ·GPIO_5 is TDO ·GPIO_6 is TRST_L
58	GND	-	-	-	-
59	GND	-	-	-	-
60	GND	-	-	-	-
61	GND	-	-	-	-
62	NC/RF_SW_CTRL8	O	-	RF_SW_CTRL8	For external antenna diversity control, Just leave it open, if the antenna diversity is not used.
63	NC	NC	-	-	-
64	NC	NC	-	-	-
65	NC	NC	-	-	-
66-72	GND	-	-	-	-

"type" Column: I=Input, O=Output, IO=Bi-directional, P=Power supply input, IL= Input signals with weak internal pull-down, IH= Input signals with weak internal pull-up, I/OH= A digital bidirectional signal, with a weak internal pull-up

7. INTERFACES TIMING

7.1 SDIO V3.0

The BM-28 WLAN section supports SDIO version 3.0 for all 1.8V 4-bit UHS-I modes:

•DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes (3.3V signaling).
•HS: High-speed up to 50 MHz (3.3V signaling).
•SDR12: SDR up to 25 MHz (1.8V signaling).
•SDR25: SDR up to 50 MHz (1.8V signaling).
•SDR50: SDR up to 100 MHz (1.8V signaling).
•SDR104: SDR up to 208MHz (1.8V signaling)
•DDR50: DDR up to 50 MHz (1.8V signaling).

The BM-28 has the ability to map the interrupt signal onto a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface.

SD 4-Bit Mode	SD 1-Bit Mode
DATA0 Data line 0	DATA Data line
DATA1 Data line 1 or Interrupt	IRQ Interrupt
DATA2 Data line 2 or Read Wait	RW Read Wait
DATA3 Data line 3	N/C Not used
CLK Clock	CLK Clock
CMD Command line	CMD Command line

Note: Per SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

7.1.1 SDIO DEFAULT MODE TIMING

SDIO default mode timing is shown by the combination of Figure 2 and table.

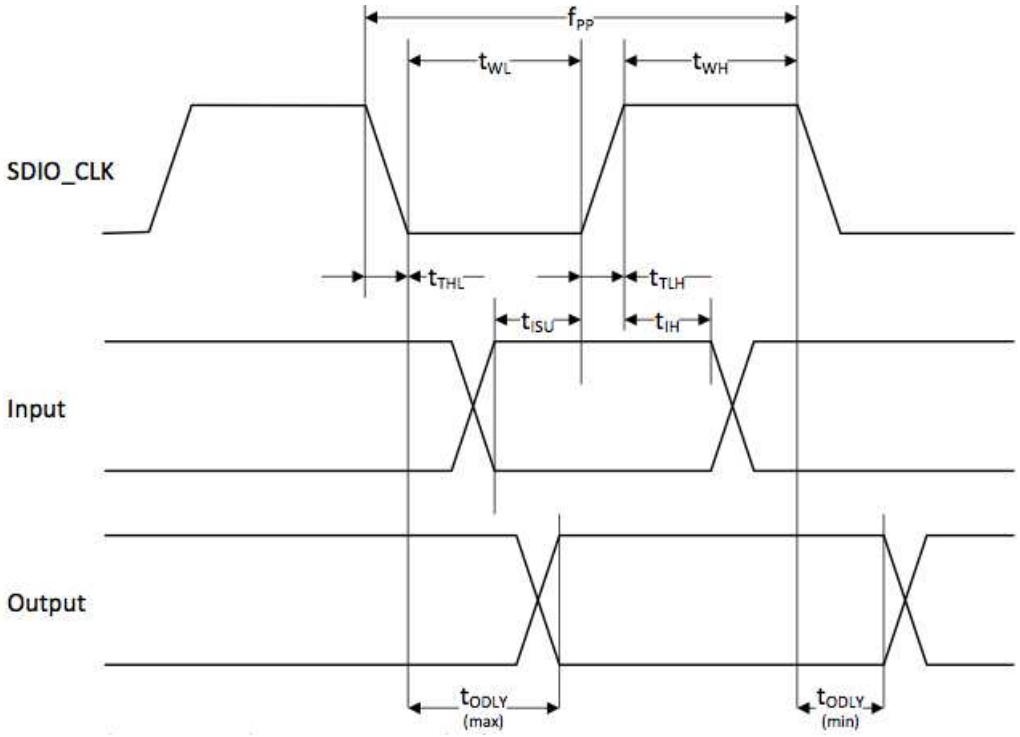


Figure 2 SDIO Bus Timing (Default Mode)

Parameter	Symbol	Min	Typical	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL)					
Frequency Data Transfer mode	fPP	0	-	25	MHz
Frequency Identification mode	fOD	0	-	400	KHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISH	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time Data Transfer mode	tODLY	0	-	14	ns
Output delay time Identification mode	tODLY	0	-	50	ns

Timing is based on CL ≤ 40pF load on CMDand Data
Min(Vih) = 0.7 x VIO and max(Vil) = 0.2 VIO

7.1.2 SDIO HIGH-SPEED MODE TIMING

SDIO default mode timing is shown by the combination of Figure 3 and table.

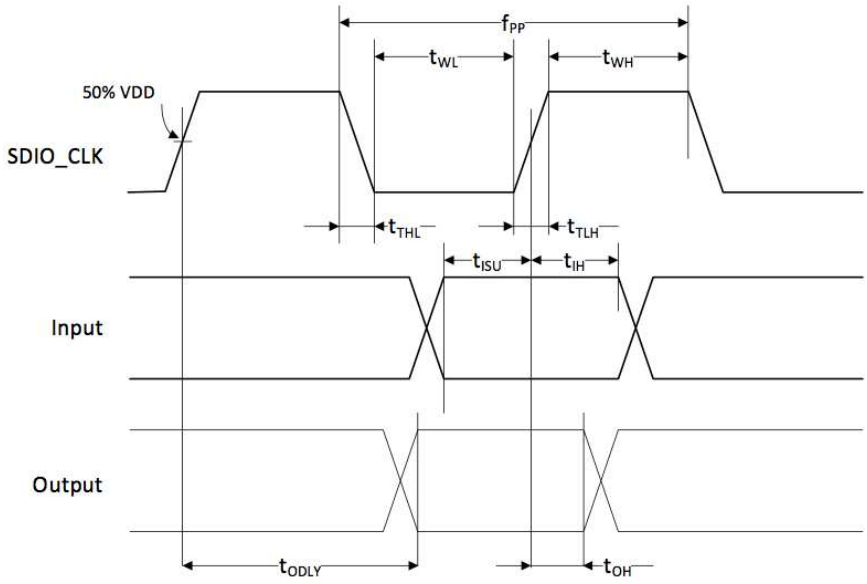


Figure 3 SDIO Bus Timing (High-Speed Mode)

Parameter	Symbol	Min	Typical	Max	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL)					
Frequency Data Transfer mode	fPP	0	-	50	MHz
Frequency Identification mode	fOD	0	-	400	KHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISH	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time Data Transfer mode	tODLY	0	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

7.1.3 SDIO BUS TIMING SPECIFICATIONS IN SDR MODES

SDR clock timing is shown by the combination of Figure 4 and table.

Clock Timing

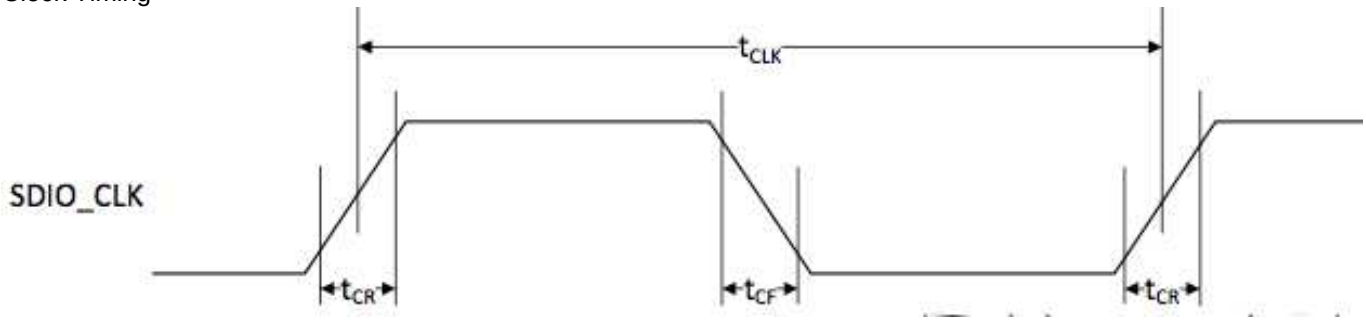


Figure 4: SDIO Clock Timing (SDR Modes)

Parameter	Symbol	Min.	Max.	Unit	Comments
-	tCLK	40	-	ns	SDR12 mode
		20	-	ns	SDR25 mode
		10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 nide
-	tCR, tCF	-	0.2 x tCLK	ns	tCR, tCF < 2.00ns (msx) @100MHz, CCARD =10pF tCR, tCF < 0.96ns (msx) @208MHz, CCARD =10pF
Clock duty	-	30	70	%	-

SDR card input timing is shown by the combination of Figure 5 and table.

7.1.4 CARD INPUT TIMING

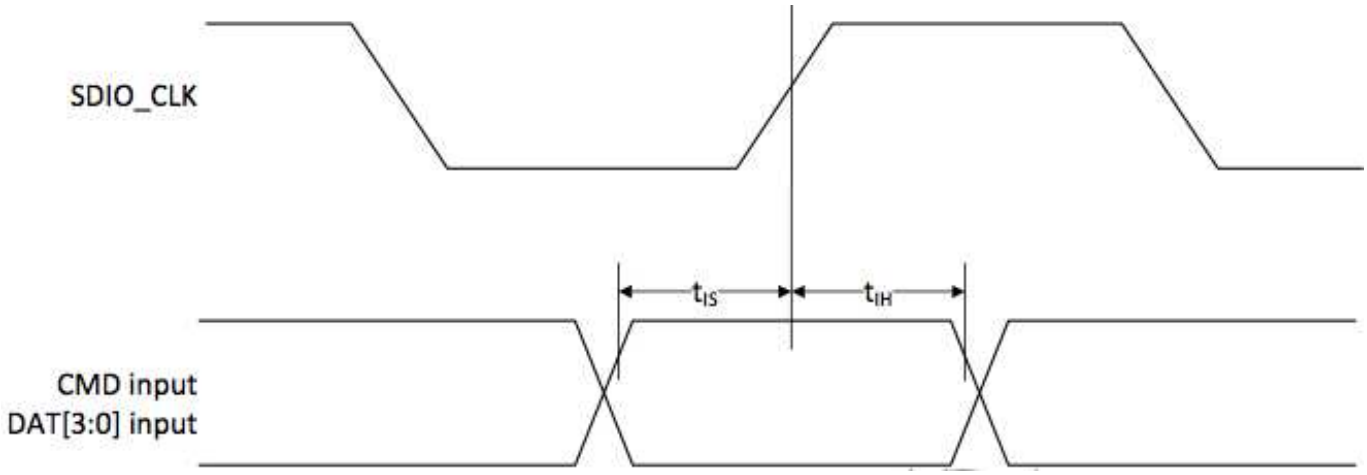


Figure 5: SDIO Bus Input Timing (SDR Modes)

Symbol	Min.	Max.	Unit	Comments
SDR104 Mode				
tIS	1.70	-	ns	C_{card} = 10pF, VCT = 0.975V
tIH	0.80	-	ns	C_{card} = 5pF, VCT = 0.975V
SDR50 Mode				
tIS	3.00	-	ns	C_{card} = 10pF, VCT = 0.975V
tIH	0.80	-	ns	C_{card} = 5pF, VCT = 0.975V

SDR card output timing is shown by the combination of Figure 6 and table.

7.1.5 CARD OUTPUT TIMING

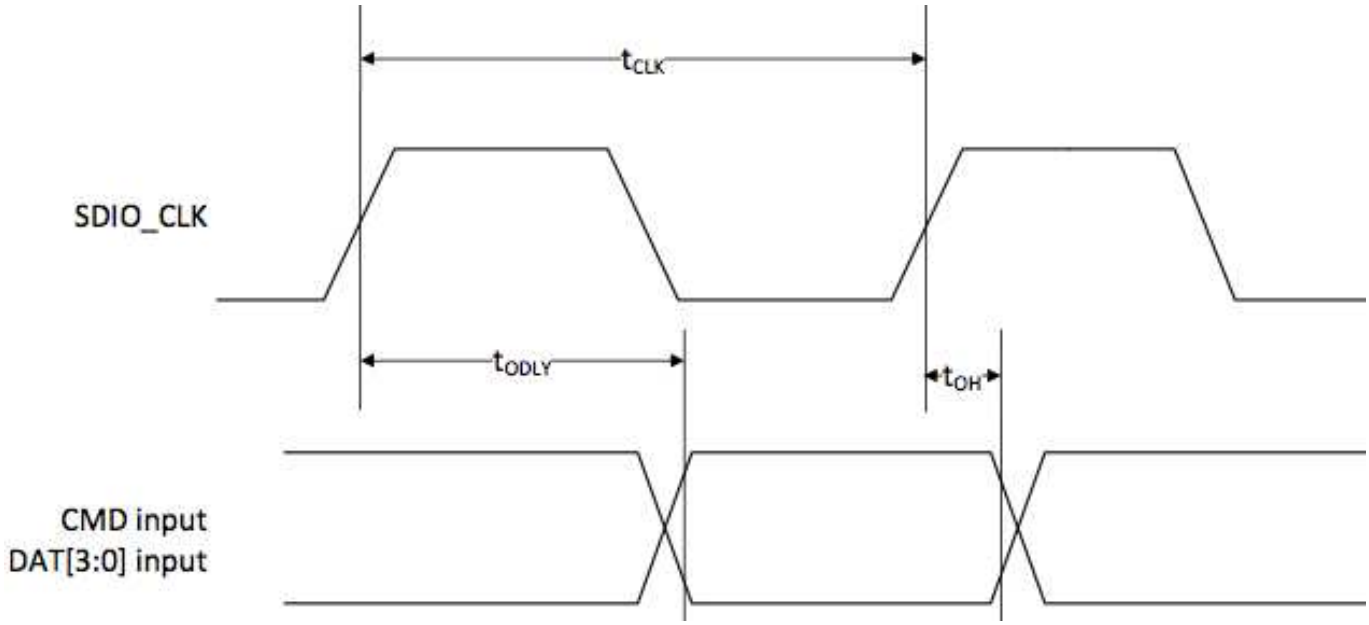
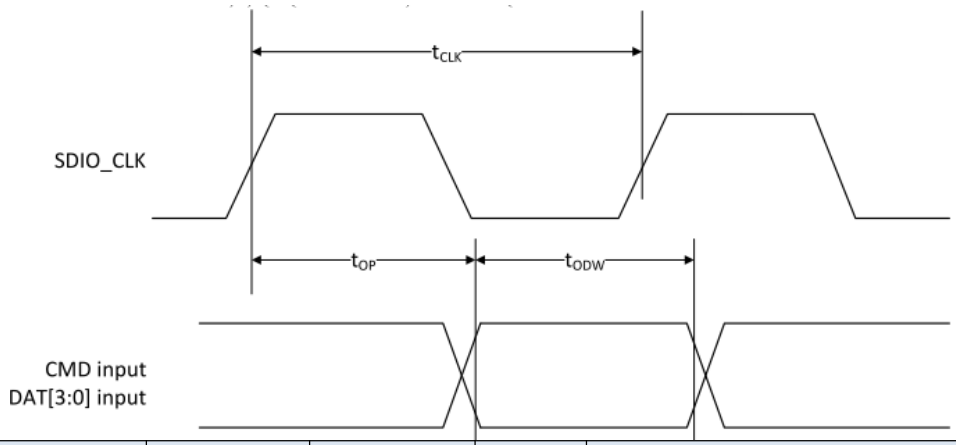


Figure 7: SDIO Bus Output Timing (SDR Modes up to 100 MHz)

Symbol	Min.	Max.	Unit	Comments
tODLY	-	9.5	ns	tCLK>= 10ns CL= 30pF using driver type B for SDR50
tODLY	-	14.0	ns	tCLK >= 20ns CL = 40pF using for SDR12, SDR25
tOH	1.5	-	ns	Hold time at the tODLY (min) CL = 15pF

Figure 7.1 SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)



Symbol	Min.	Max.	Unit	Comments

t_{OP}	**0**	**2**	**UI**	Card output phase
Δt_{OP}	**-350**	**+1550**	**ps**	Delay variation due to temp change after tuning
t_{ODW}	**0.6**	**-**	**UI**	t_{ODW}=2.88 ns @208 MHz

7.1.6 SDIO BUS TIMING SPECIFICATIONS IN DDR50 MODE

DDR50 clock timing is shown by the combination of Figure 7 and table.

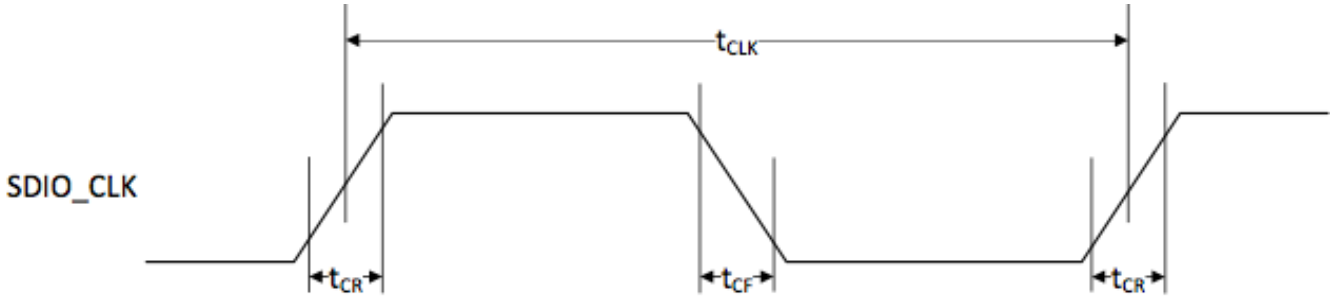


Figure 7: SDIO Bus Clock Timing (DDR50 Mode)

Parameter	Symbol	Min.	Max.	Unit	Comments
-	tCLK	20	-	ns	DDR50 mode
-	tCR, tCF	-	0.2 x tCLK	ns	tCR, TcF <4.00 ns (max) @50MHz, Ccard = 10pF
Clock Duty	-	45	55	%	-

7.1.7 DATA TIMING

DDR50 data timing is shown by the combination of Figure 8 and table.

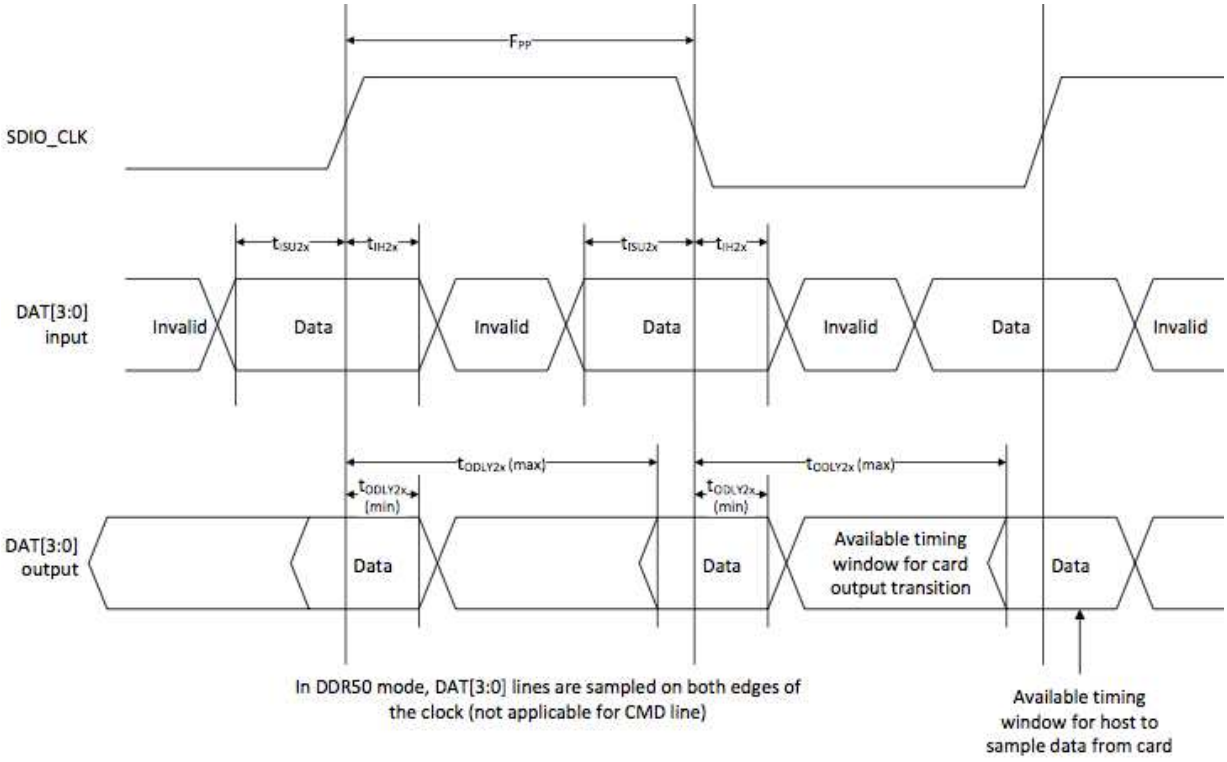


Figure 8: SDIO Bus Data Timing (DDR50 Mode)

Parameter	Symbol	Min.	Max.	Unit	Comments
Input CMD					
Input setup time	tISU	6	-	ns	Ccard < 10pF (1 Card)
Input hold time	tIH	0.8	-	ns	Ccard < 10pF (1 Card)
Output CMD					
Output delay time	tODLY	-	13.7	ns	Ccard < 30pF (1 Card)
Output hold time	tOH	1.5	-	ns	Ccard < 15pF (1 Card)
Input DAT					
Input setup time	tISU2x	3	-	ns	Ccard < 10pF (1 Card)
Input hold time	tIH2x	0.8	-	ns	Ccard < 10pF (1 Card)
Output DAT					
Output delay time	tODLY2x	-	7.5	ns	Ccard < 25pF (1 Card)
Output hold time	tODLY2x	1.5	-	ns	Ccard < 15pF (1 Card)

8. BLUETOOTH PERIPHERAL TRANSPORT UNIT

8.1 SPI INTERFACE

The BM-28 supports a slave SPI HCI transport with an input clock range of up to 16 MHz. Higher clock rates can be possible. The physical interface between the SPI master and BM-28 consists of the four SPI signals (SPI_CSB, SPI_CLK, SPI_SI, and SPI_SO) and one interrupt signal (SPI_INT). The SPI signals are muxed onto the UART signals, see Table below.

SPI Signals	*UART Signals*
SPI_CLK	**UART_CTS_N**
SPI_CSB	**UART_RTS_N**
SPI_MISO	**UART_TXD**
SPI_MOSI	**UART_RXD**
SPI_INT	**BT_DEV_WAKE**

8.1.1 SPI/UART TRANSPORT DETECTION

The BT_HOST_WAKE pin is also used for BT transport detection. The transport detection occurs during the power-up sequence. It selects either UART or SPI transport operation based on the following pin state:

- If the BT_HOST_WAKE pin is pulled low by an external pull-down during power-up, it selects the SPI transport interface.
- If the BT_HOST_WAKE pin is not pulled low externally during power-up, then the default internal pull-up is detected as a high and it selects the UART transport interface.

8.2 UART INTERFACE

The BM-28 uses a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command

UART timing is shown by the combination of Figure 10 and table.

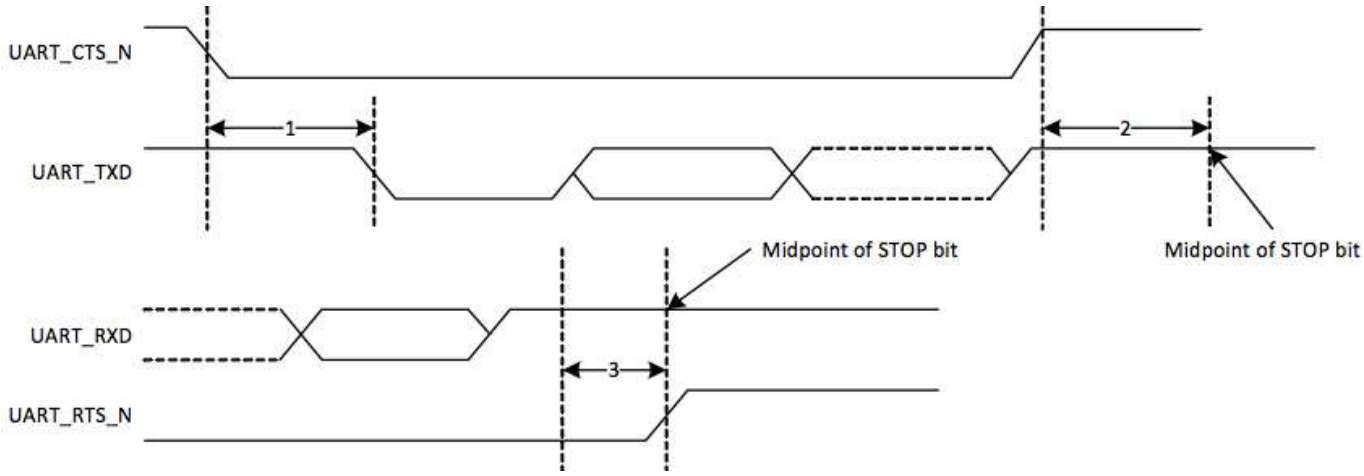


Figure 10: UART Timing

Ref NO.	Characteristics	Min.	Typical	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	-	-	0.5	Bit periods

8.3 I²S INTERFACE

The BM-28I supports two independent I²S digital audio ports: one for Bluetooth audio, and one for high-fidelity FM audio. The I²S interface for FM audio supports both master and slave modes. The I²S signals are:
I²S clock: I²S SCK
I²S Word Select: I²S WS
I²S Data Out: I²S SDO
I²S Data In: I²S SDI

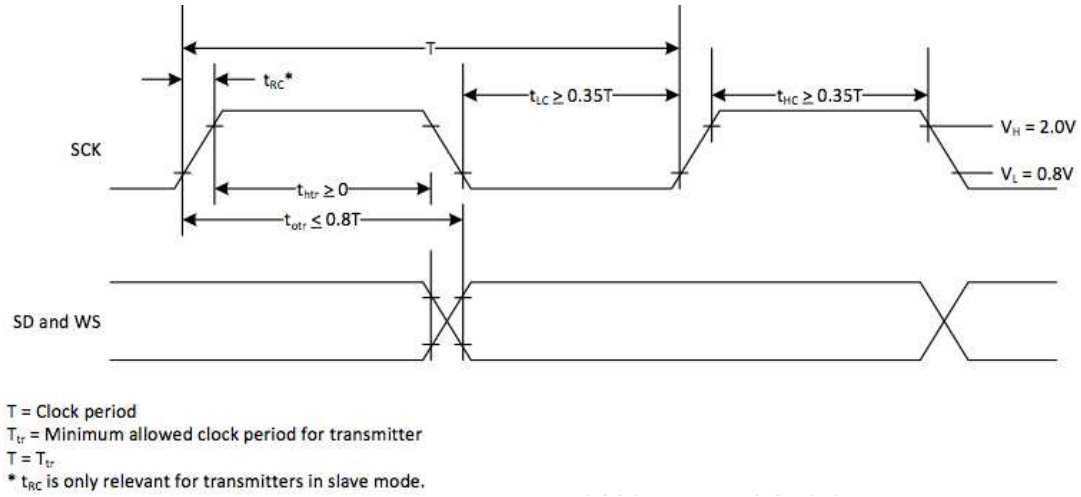


Figure 11: I²S Transmitter Timing

Transmitter				
	Lower Limit		Upper Limit	
	Min.	Max.	Min.	Max.
Clock Period T	Ttr	-	-	-
Master Mode: Clock generated by transmitter or receiver				
HIGH tHC	0.35Ttr	-	-	-
LOW tLC	0.35Ttr	-	-	-
Slave Mode: Clock generated by transmitter or receiver				
HIGH tHC	-	0.35Ttr	-	-
LOW tLC	-	0.35Ttr	-	-
Rise time tRC	-	-	0.15Ttr	-
Transmitter				
Delay tdtr	-	-	-	0.8T
Hod time thtr	0	-	-	-

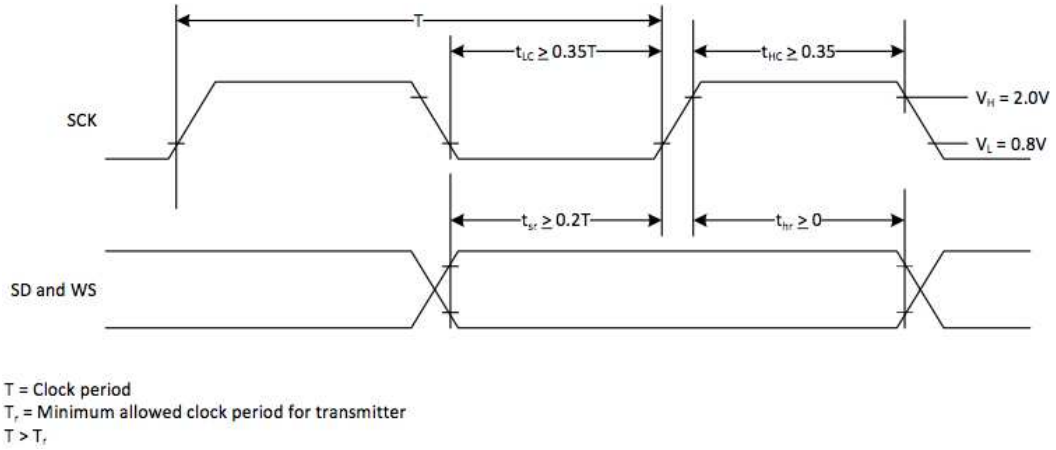


Figure 12: I²S Receiver Timing

Receiver				
	Lower Limit		Upper Limit	
	Min.	Max.	Min.	Max.
Clock Period T	Ttr	-	-	-
Master Mode: Clock generated by transmitter or receiver				
HIGH tHC	0.35Ttr	-	-	-
LOW tLC	0.35Ttr	-	-	-
Slave Mode: Clock generated by transmitter or receiver				
HIGH tHC	-	0.35Ttr	-	-
LOW tLC	-	0.35Ttr	-	-
Rise time tRC	-	-	-	-
Receiver				
Setup time tsr	-	0.2Tr	-	-
Hold time thr	-	0	-	-

9. LEGAL, REGULATORY & OTHER TECHNICAL CONSTRAINTS

9.1 REGULATORY COMPLIANCE

USI will do the regulatory compliance pre-test and help debug if necessary to ensure that all conducted and radiated emissions in transmit and receive modes meet the regulatory limits required by the country(s) being certified. Customers shall provide the list of applicable countries to the supplier during the development phase of the module.

9.2 POWER-UP SEQUENCE

9.2.1 WLAN = ON, BLUETOOTH = ON

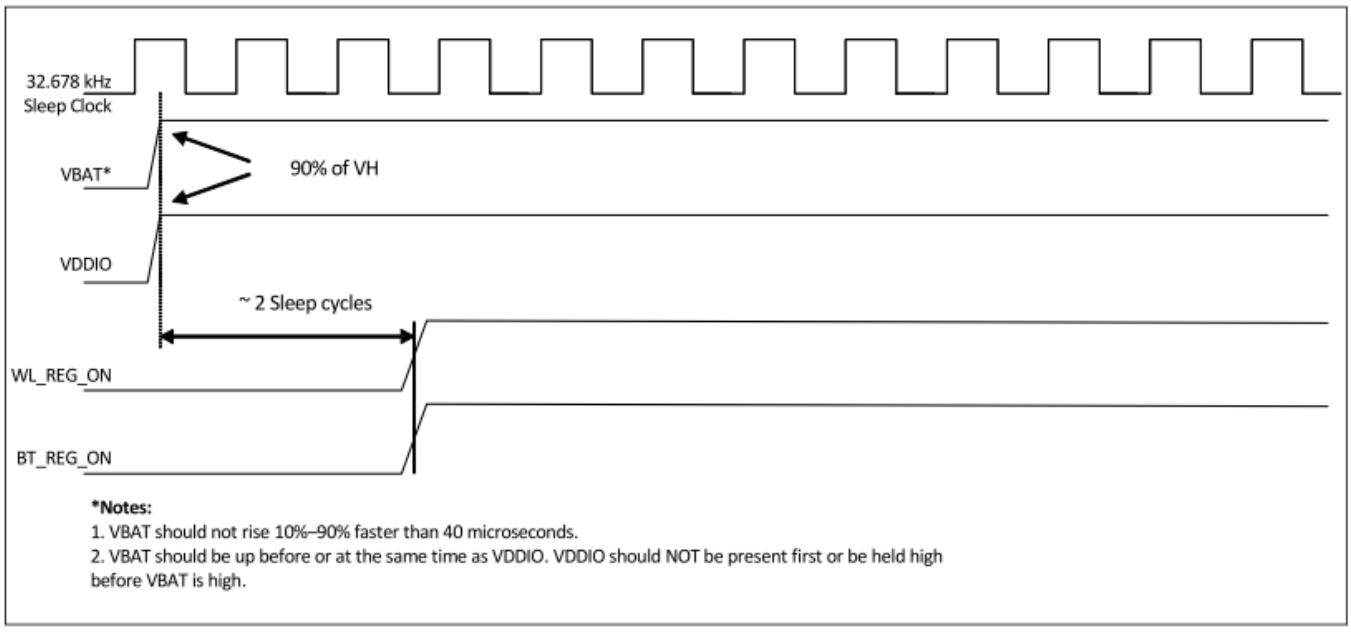


Figure 20 WLAN = ON, Bluetooth = ON

9.2.2 WLAN = OFF, BLUETOOTH = OFF

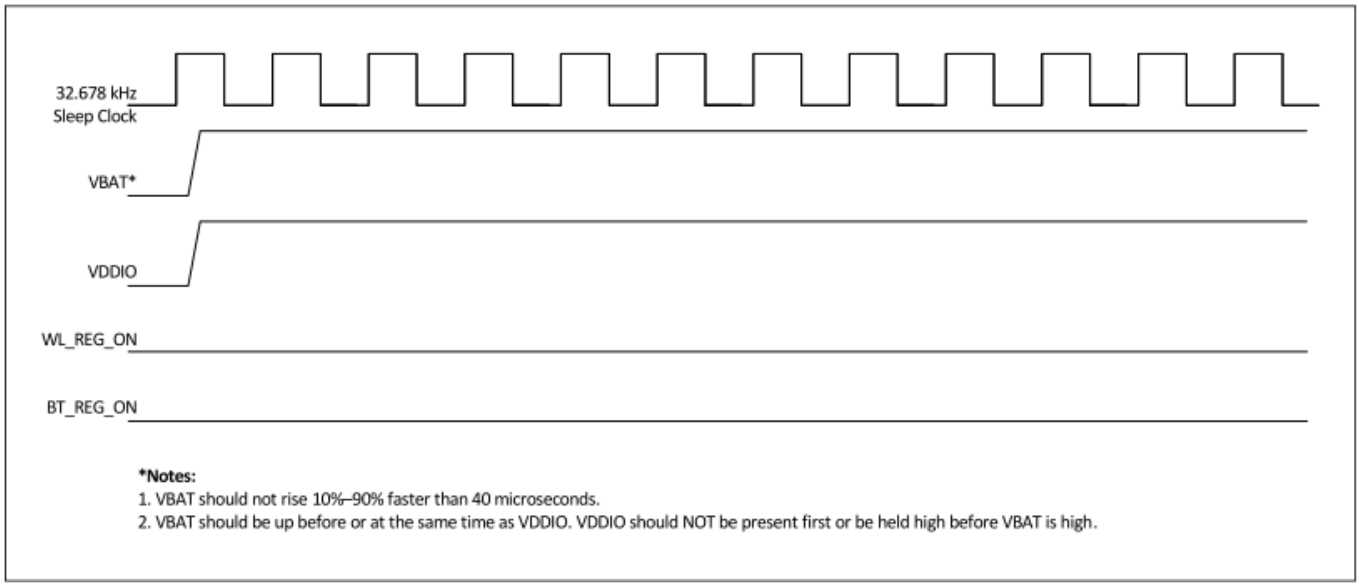


Figure 20.1 WLAN = OFF, Bluetooth = OFF

9.2.3 WLAN = ON, BLUETOOTH = OFF

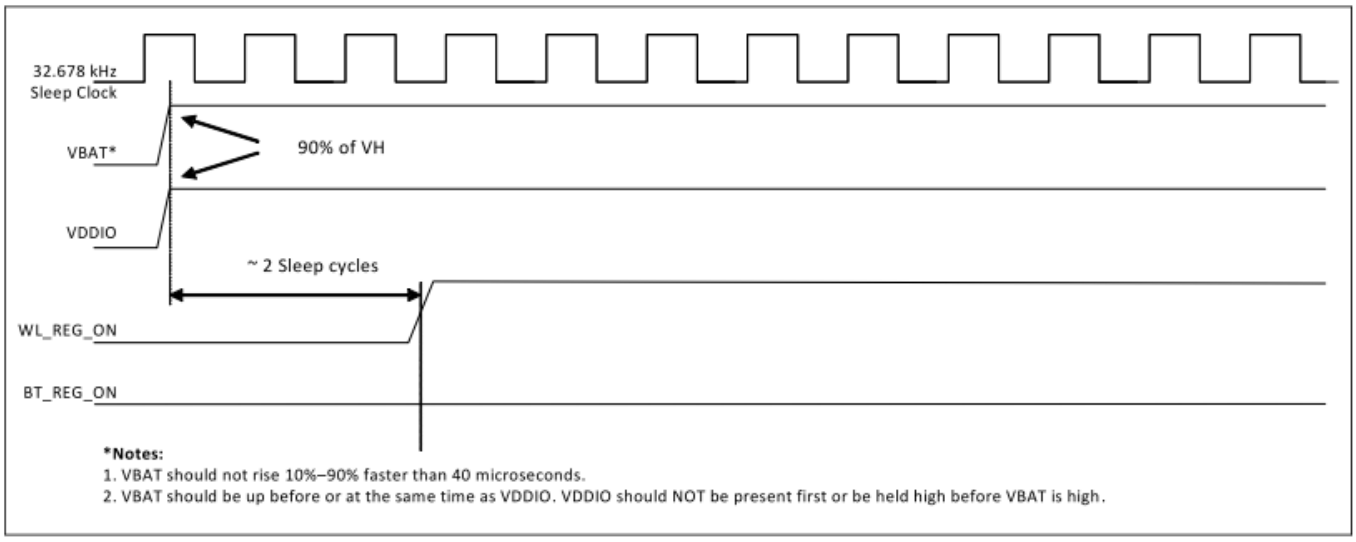


Figure 20.2 WLAN = ON, Bluetooth = OFF

9.2.4 WLAN = OFF, BLUETOOTH = ON

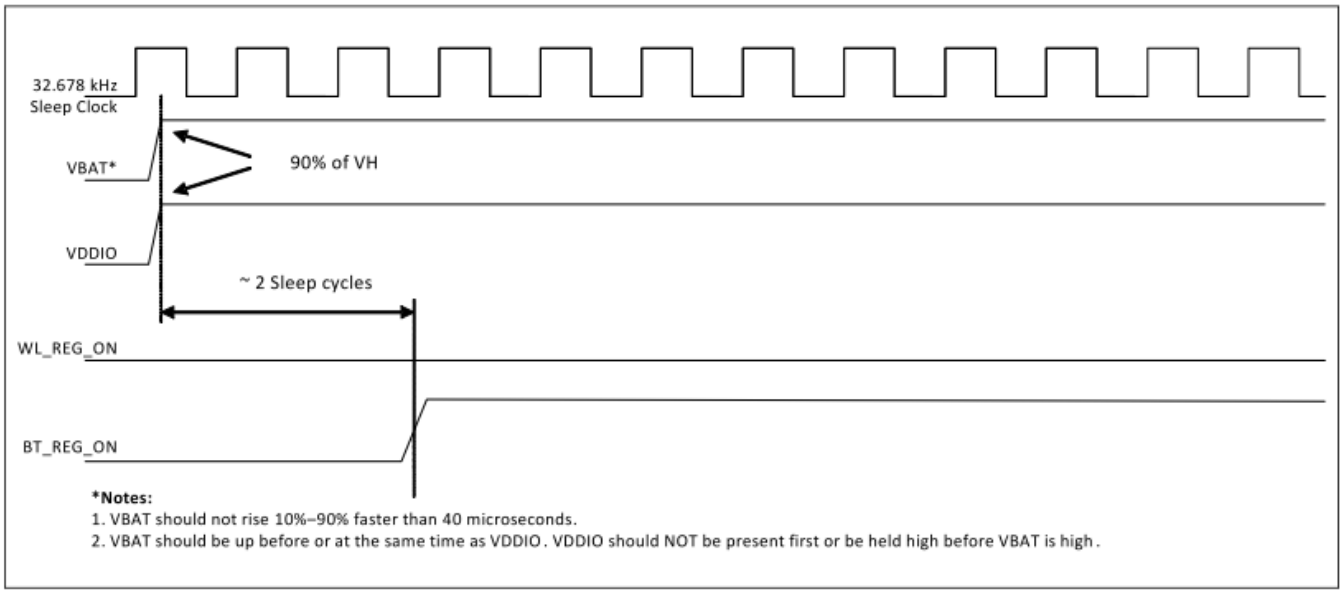
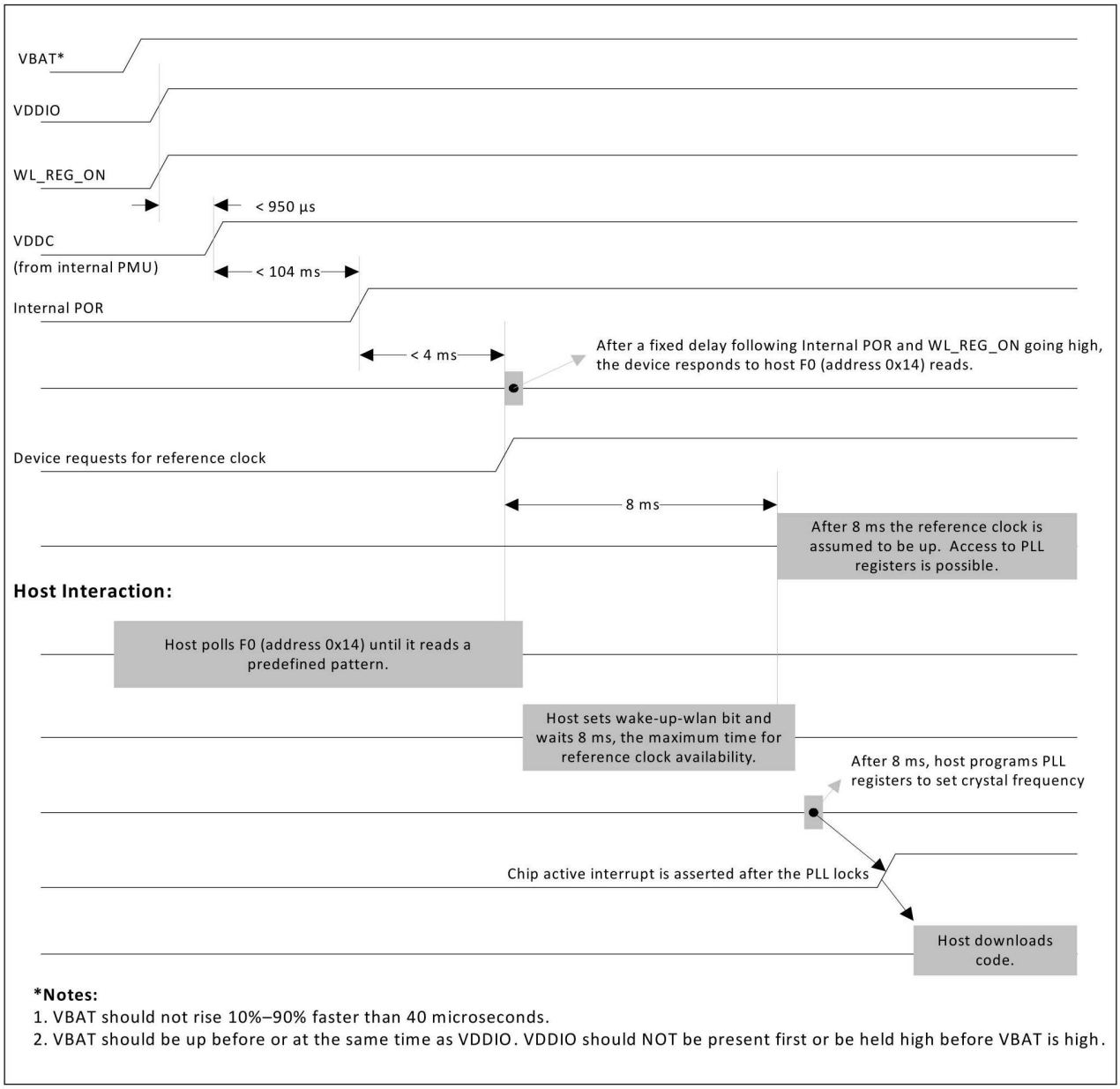


Figure 20.3 WLAN = OFF, Bluetooth = ON

9.2.5 WLAN BOOT-UP SEQUENCE



***Notes:**

1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

9.3 EXTERNAL 32.768 KHZ LOW-POWER OSCILLATOR

The BM-28 uses a secondary low-frequency clock for low-power-mode timing. Either the internal low- precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some WLAN applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-200	ppm
Duty cycle	30-70	%
Input signal amplitude	0.2-3.3	v, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k	ohm
Capacitive	<5	pF
Clock jitter (integrated over 300 Hz–15 kHz)	<5	ns
Clock jitter (during initial start-up)	<10000	ppm

9.4 WLAN/BT GPIO SIGNALS AND STRAPPING OPTIONS

Pin Name	*Default Pull During Strapping*	*All Packages*
GPIO_7	0	JTAG_ENABLE
GPIO_16	1	VTRIM_EN
GPIO_17	1	SDIO_PADVDDIO: 0 ≥ 3.3V, 1 ≥ 1.8V; when SDIO is enabled (strap from GPIO_18 is 0). SPROM_ABSENT: 0 ≥ SPROM present, 1 ≥ SPROM absent; when SDIO is disabled (strap from GPIO_18 is 1).
GPIO_18	1	SDIO_DISABLE: 0 ≥ SDIO enabled, 1 ≥ SDIO disabled; either PCIe or SDIO or both have to be present.
GPIO_19	1	PCIE_ENABLE: 0 ≥ PCIe disabled, 1 ≥ PCIe enabled; either PCIe or SDIO or both have to be present.

9.4.1 HOST INTERFACE SELECTION

Note: The strapping options are defined in such a way that defaults have internal pull-ups, so that it is easy to configure the strap value in opposite manner on a board (put a pull-down on the board).

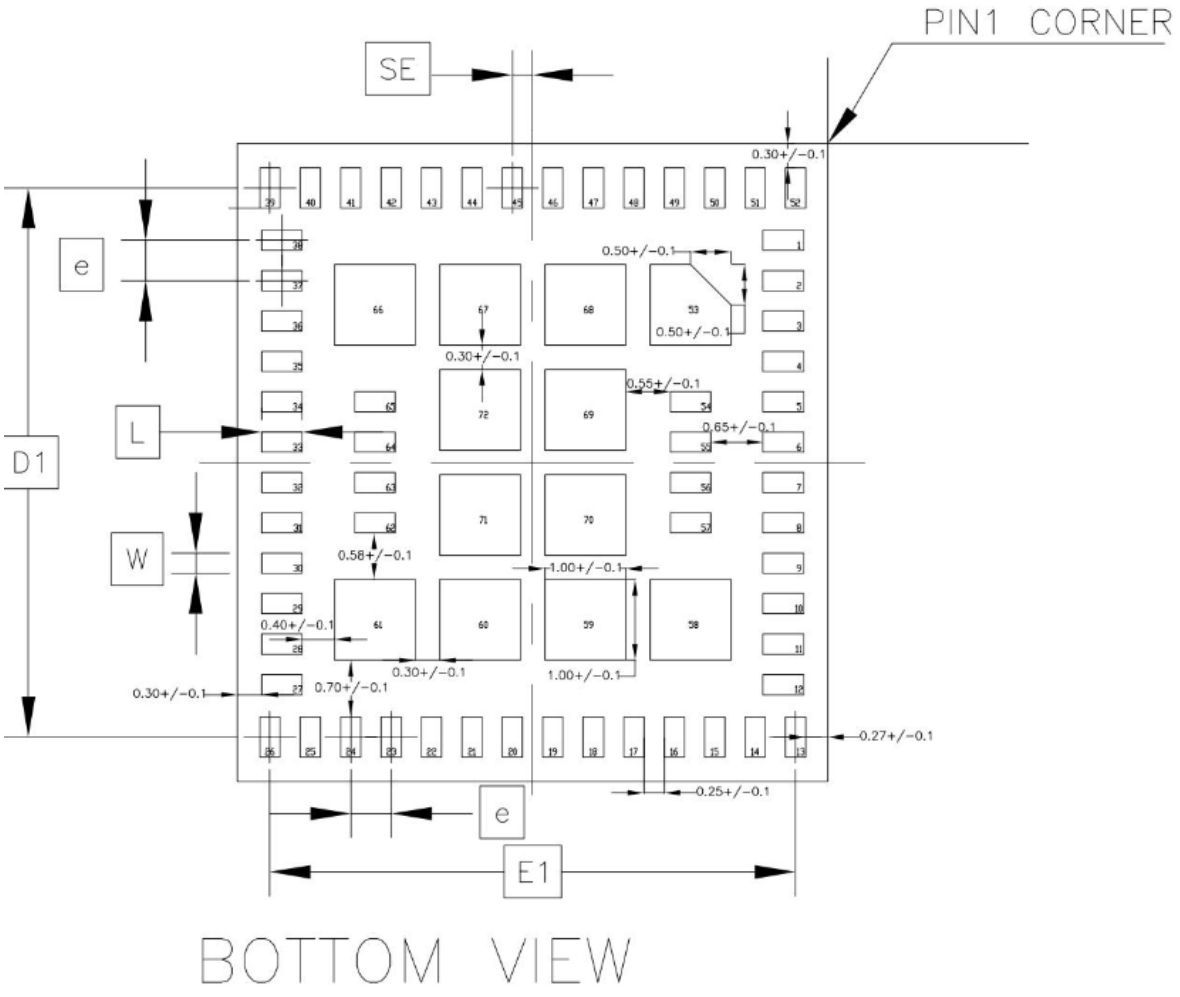
Host Interface Selection

PCIe Enable	*SDIO Disable*	*SDIO PADVDDIO/ SPROM Absent*	*Mode*
1	1	1	PCIe
1	1	0	PCIe + SPROM
0	0	1	1.8V SDIO
0	0	0	3.3V SDIO
1	0	1	PCIe + SDIO(1.8V)
1	0	0	PCIe + SDIO (3.3V)

10. ASSEMBLY RECOMMENDATIONS

10.1 FOOT PRINT

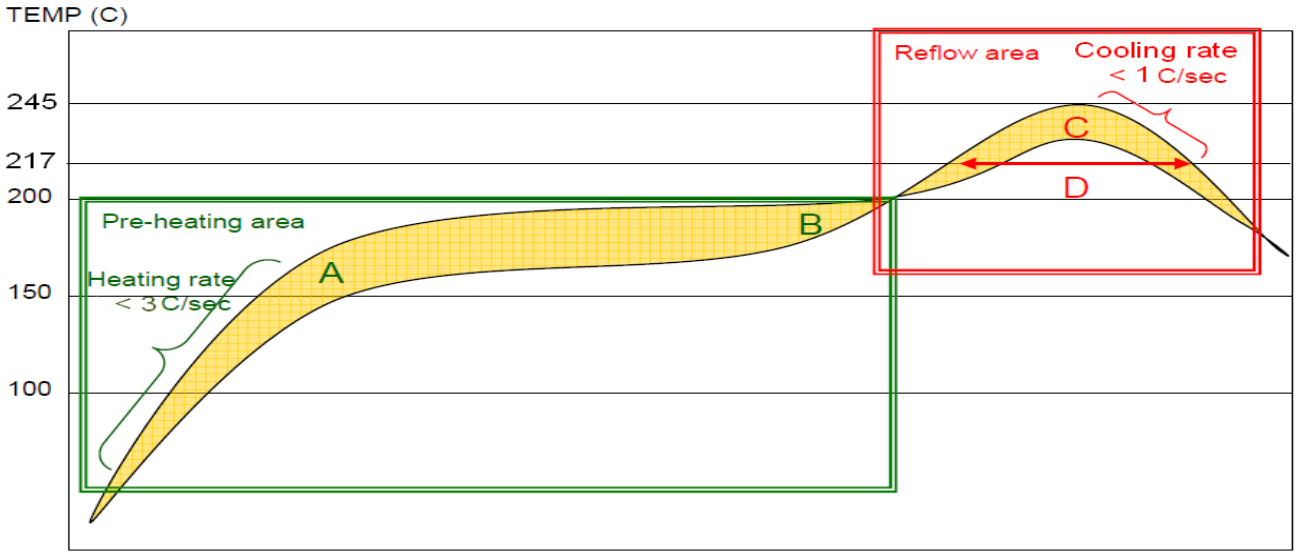
Unit: mm



	Symbol	Common Dimensions		
		MIN.	NOM.	MAX.
Package :	PIM	---		
Ball Pitch :	e	0.500		
Lead Width	W	0.150	0.250	0.350
Lead Length	L	0.400	0.500	0.600
BODY CENTER TO CONTACT BALL	SE	0.246		
Package Edge Tolerance :	aaa	0.100		
Lead Count :	n	72		
EDGE BALL CENTER TO CENTER:	D1	6.800		
	E1	6.500		

Figure 21 Recommended Landing Pads Design for Module (TOP VIEW)

11. RECOMMENDED REFLOW PROFILE



(1) Solder paste alloy : SAC305 (Sn96.5/Ag3.0/Cu0.5) (Lead Free solder paste.)
(2) A-B. Temp.: 150~200℃; soak time:60~120sec.(Base on Flux type, reference only)
(3) C. Peak temp: <245℃
(4) D. Time above 217 ℃: 40~90sec.(Base on SAC305)
(5) Suggestion: Optimal cooling rate is <1℃/sec. from peak to 217 ℃.
(6) Nine heater zones at least for Reflow equipment.
(7) Nitrogen usage is recommended and be controlled the value less than 1500 ppm.
Note: Need to inspect solder joint by X-ray post reflow

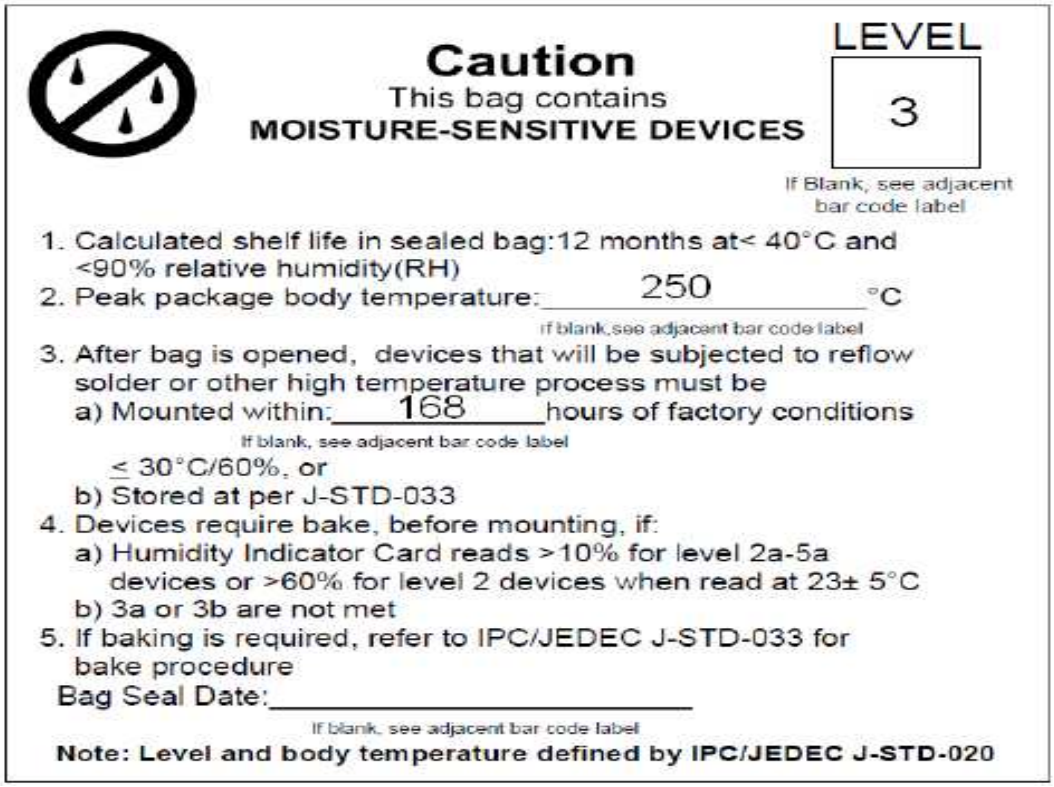
12. PACKAGE AND STORAGE CONDITION

12.1 PACKAGE & TAPE REEL DIMENSION

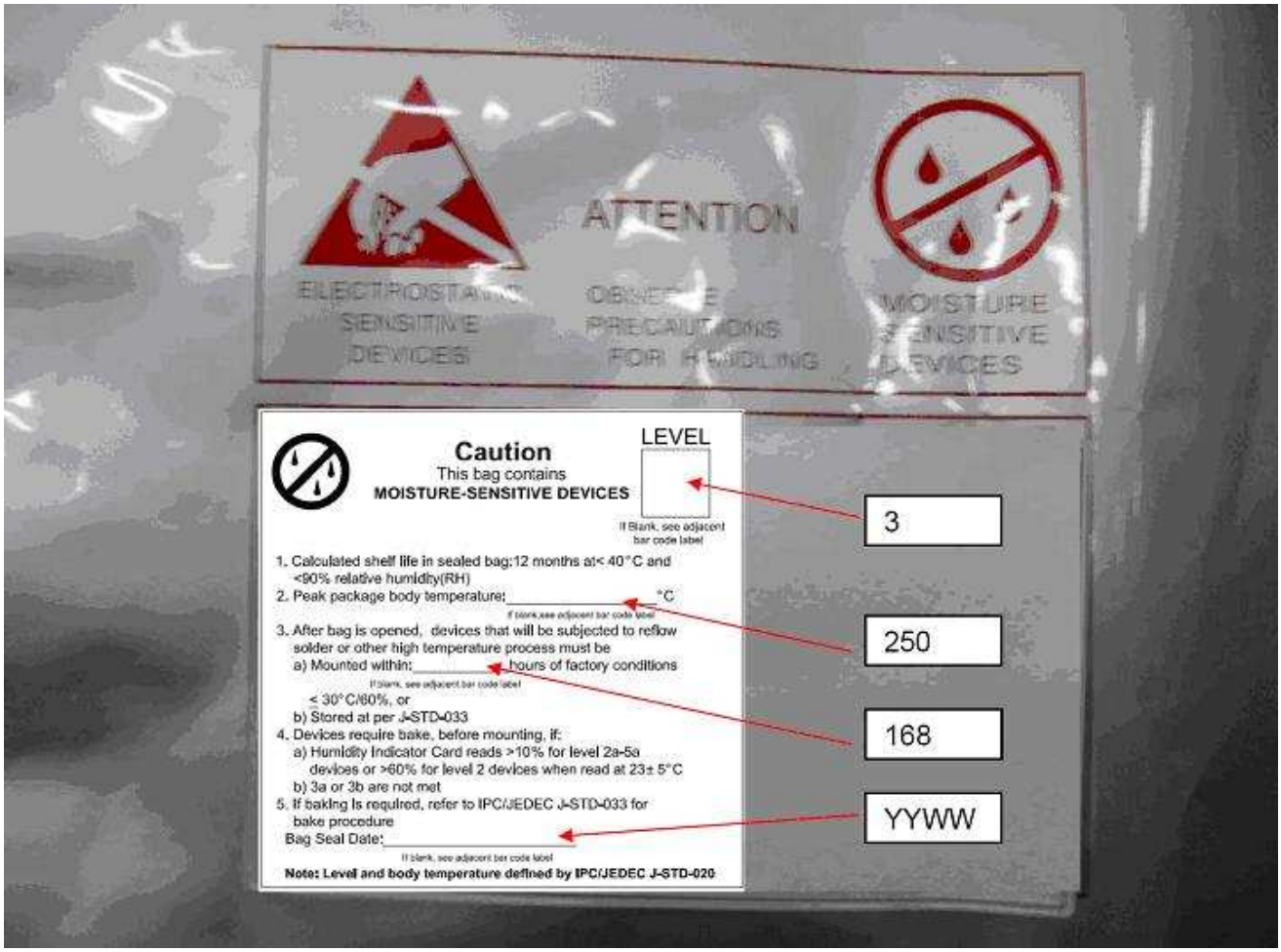
12.2 ESD LEVEL

1. Surface Resistively:
   Interior:109~1011Ω/SQUARE
   EXTERIOR:108~1012Ω/SQUARE
2. Dimension:480*420mm
3. Tolerance:+5,0mm
4. Color:
   Background : Gray
   Text : Red

12.3 MSL Level/Storage condition



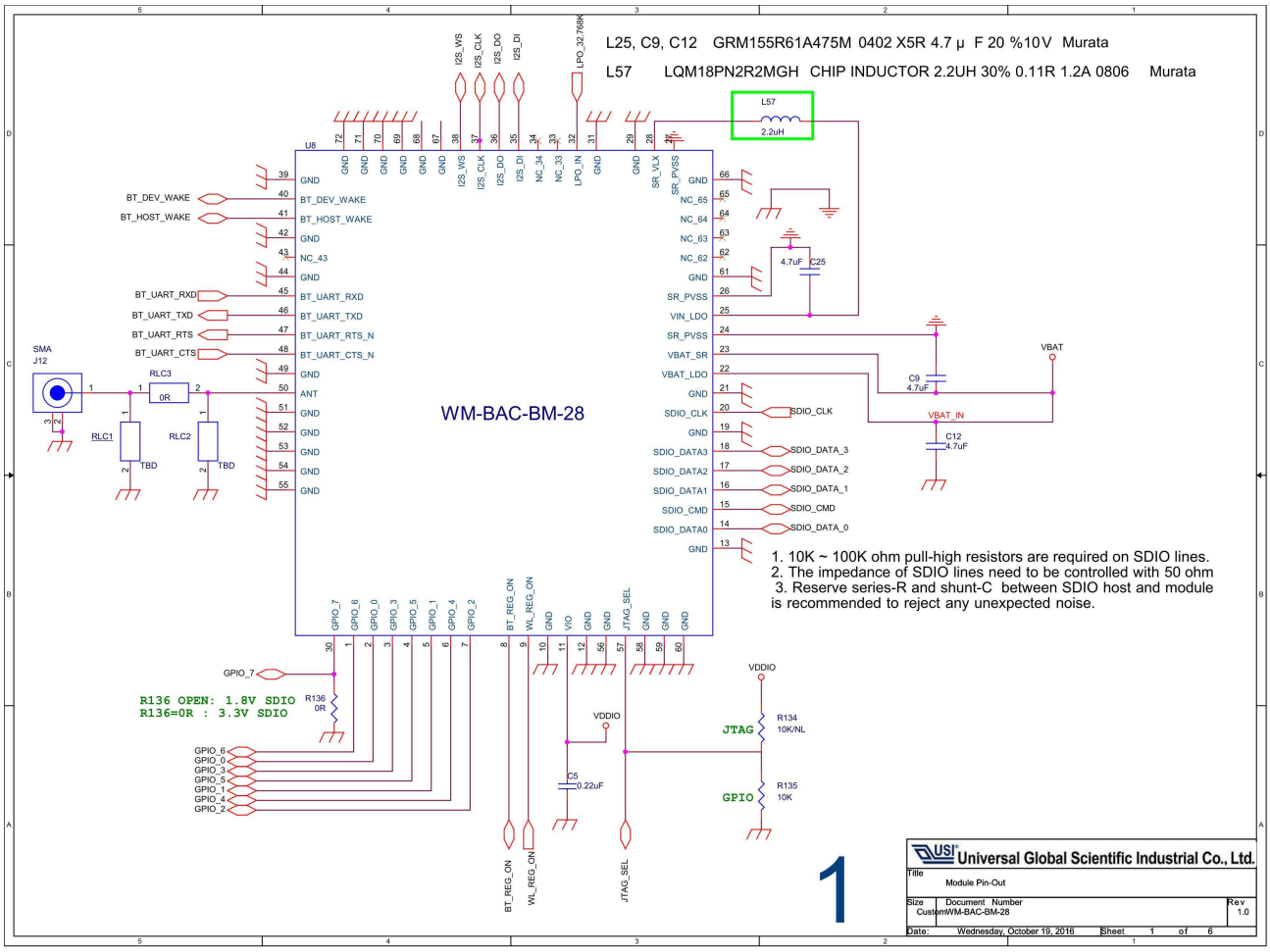
12.3 MOISTURE SENSITIVE LABEL



Life Cycle: 2 year
Extra TC Check Point: TC750, TC1000

13. APPLICATION REFERENCE DESIGN

13.1 SDIO SCHEMATIC



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